2.5V/3.3V DUAL 1:5 DIFFERENTIAL LVECL/LVPECL/HSTL CLOCK DRIVER

Precision Edge® SY100EP210U

FEATURES

- 2.5V and 3.3V power supply options
- Guaranteed AC parameters over temperature:
  - f_{MAX} > 3.0GHz
  - < 25ps within-device skew
  - < 250ps t_r / t_f
  - < 380ps propagation delay (differential)
- Wide temperature range: –40°C to +85°C
- Differential design
- V_{BB} output
- Fully compatible with industry standard 100K I/O levels
- Available in 32-pin TQFP Package

Precision Edge®

DESCRIPTION

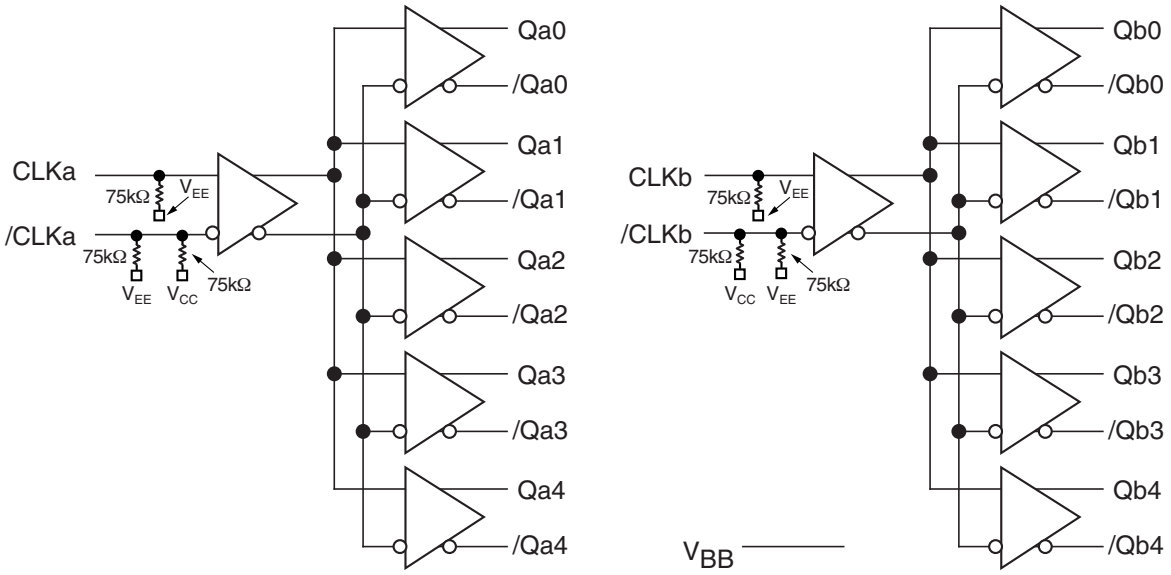
The SY100EP210U is a high-speed, precision low skew 1-to-5 dual differential clock driver. HSTL inputs can be used when the EP210U is operating in PECL mode.

The EP210U specifically guarantees critical AC parameters over temperature and voltage. Optimal design, layout, and processing minimize skew within device and from device-to-device.

The SY100EP210U, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the EP210U to be used for high performance clock distribution in +3.3V or +2.5V systems. Single-ended input operation is limited to a $V_{CC} \geq 3.0V$ in PECL mode, or $V_{EE} \leq -3.0V$ in ECL mode.

Designers can take advantage of the EP210U's performance to distribute low skew clocks across the backplane or to multiple points on a board.

BLOCK DIAGRAM



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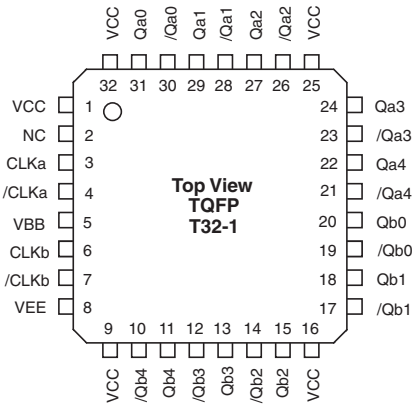
PACKAGE/ORDERING INFORMATION



32-Pin TQFP (T32-1)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100EP210UTC	T32-1	Commercial	XEP210U	Sn-Pb
SY100EP210UTCTR[2]	T32-1	Commercial	XEP210U	Sn-Pb
SY100EP210UTG[3]	T32-1	Industrial	XEP210U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY100EP210UTGTR[2, 3]	T32-1	Industrial	XEP210U with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN NAMES

Pin	Function
CLKa, /CLKa	LVPECL, LVECL, HSTL Clock Input: CLKa input includes a 75kΩ pull-down. Default is LOW if left floating. /CLKa includes both pull-up and pull-down resistors. Default condition is V_{CC}/2.
CLKb, /CLKb	LVPECL, LVECL, HSTL Clock Input: CLKb input includes a 75kΩ pull-down. Default is LOW if left floating. /CLKb includes both pull-up and pull-down resistors. Default condition is V_{CC}/2.
Qn0:4, /Qn0:4	LVPECL or LVECL Outputs: Terminate to V_{CC}–2V. (see “Termination” section)
V_{BB}	Reference Voltage for Single-Ended Inputs: It provides the switching reference for the input differential amplifier. When used, bypass with a 0.0μF capacitor to the most positive reference (usually V_{CC}) as shown in Figure 3.
V_{CC}	Positive Power Supply: For LVPECL operation, connect V_{CC} to 3.3V or 2.5V. For LVECL operation, connect to GND. Bypass with 0.1μF//0.01μF low ESR capacitors.
V_{EE}	Negative Power Supply: For LVPECL operation, connect to GND. For LVECL operation, connect to –3.3V or –2.5V.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{CC} — V_{EE}	Power Supply Voltage		6.0	V
V_{IN}	Input Voltage (V_{CC} = 0V, V_{IN} not more negative than V_{EE}) Input Voltage (V_{EE} = 0V, V_{IN} not more positive than V_{CC})		–6.0 to 0 +6.0 to 0	V V
I_{OUT}	Output Current	–Continuous –Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current[2]		±0.5 to 0	mA
T_{LEAD}	Lead Temperature (soldering, 20sec.)		+260	°C
T_A	Operating Temperature Range		–40 to +85	°C
T_{store}	Storage Temperature Range		–65 to +150	°C
θ_{JA}	Package Thermal Resistance (Junction-to-Ambient)	–Still-Air –500lfpm	50 42	°C/W
θ_{JC}	Package Thermal Resistance (Junction-to-Case)		20	°C/W

Note 1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.

Note 2. Use for inputs of same package only.

DC ELECTRICAL CHARACTERISTICS[1]

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{CC}	Power Supply (LVPECL) Voltage (LVECL)	2.37 –2.37	— —	3.8 –3.8	2.37 –2.37	— —	3.8 –3.8	2.37 –2.37	— —	3.8 –3.8	V	
I_{EE}	Internal Supply Current	—	70	90	—	70	90	—	70	90	mA	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	$V_{IN} = V_{IH}$
I_{IL}	Input LOW Current CLKa, CLKb /CLKa, /CLKb	 0.5 –150	 — —	 — —	 0.5 –150	 — —	 — —	 0.5 –150	 — —	 — —	 µA µA	 V_{IN} = 0V V_{IN} = 0V
C_{IN}	Input Capacitance	—	—	—	—	2	—	—	—	—	pF	

Note 1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

3.3V LVPECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 3.3V ±10%

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IH}	Input HIGH Voltage	2135	—	2420	2135	—	2420	2135	—	2420	mV	
V_{IL}	Input LOW Voltage	1490	—	1675	1490	—	1675	1490	—	1675	mV	
V_{OL}	Output LOW Voltage	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV	50Ω to V_{CC} –2V
V_{OH}	Output HIGH Voltage	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV	50Ω to V_{CC} –2V
V_{BB}	Output Reference Voltage[2]	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV	
V_{IHCMR}	Input HIGH Voltage Common Mode Range[3]	1.2	—	V_{CC}	1.2	—	V_{CC}	1.2	—	V_{CC}	mV	

Note 1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output varies 1:1 with V_{CC}.

Note 2. Single-ended input operation is limited to $V_{CC} \geq 3.0V$ in LVPECL mode. V_{BB} reference varies 1:1 with V_{CC}.

Note 3. The V_{IHCMR} (min) varies with V_{EE}. V_{IHCMR} (max) varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

2.5V LVPECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 2.5V ±10%, V_{EE} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{OL}	Output LOW Voltage	555	680	895	555	680	895	555	680	895	mV	50Ω to V_{CC} –2V
V_{OH}	Output HIGH Voltage	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV	50Ω to V_{CC} –2V
V_{IHCMR}	Input HIGH Voltage[2] Common Mode Range	1.2	—	V_{CC}	1.2	—	V_{CC}	1.2	—	V_{CC}	V	

Note 1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output varies 1:1 with V_{CC}.

Note 2. The V_{IHCMR} (min) varies with V_{EE}. V_{IHCMR} (max) varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

LVECL DC ELECTRICAL CHARACTERISTICS[1]

V_{EE} = –2.375V to –3.8V; V_{CC} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-Ended)	–1810	—	–1625	–1810	—	–1625	–1810	—	–1625	mV	
V_{IH}	Input HIGH Voltage (Single-Ended)	–1165	—	–0880	–1165	—	–0880	–1165	—	–0880	mV	
V_{OL}	Output LOW Voltage	–1945	–1820	–1695	–1945	–1820	–1695	–1945	–1820	–1695	mV	50Ω to V_{CC} –2V
V_{OH}	Output HIGH Voltage	–1145	–1020	–0895	–1145	–1020	–0895	–1145	–1020	–0895	mV	50Ω to V_{CC} –2V
V_{BB}	Output Reference Voltage[2]	–1525	–1425	–1325	–1525	–1425	–1325	–1525	–1425	–1325	mV	
V_{IHCMR}	Input HIGH Voltage Common Mode Range[3]	V_{EE} +1.2		0.0	V_{EE} +1.2		0.0	V_{EE} +1.2		0.0	V	

Note 1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

Note 2. Single-ended input operation is limited to $V_{EE} \le$ –3.0V in ECL/LVECL mode. V_{BB} reference varies 1:1 with V_{CC}.

Note 3. The V_{IHCMR} (min) varies with V_{EE}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

HSTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.375V to 3.8V; V_{EE} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IH}	Input HIGH Voltage	1200	—	—	1200	—	—	1200	—	—	mV	
V_{IL}	Input LOW Voltage	—	—	400	—	—	400	—	—	400	mV	
V_X	Input Crossover Voltage	680	—	900	680	—	900	680	—	900	mV	

AC ELECTRICAL CHARACTERISTICS

(LVPECL) V_{CC} = 2.375 to 3.8V, V_{EE} = 0V; (LVECL) V_{EE} = –2.375V to –3.8V, V_{CC} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Maximum Frequency(1) HSTL/LVPECL	3.0	—	—	3.0	—	—	3.0	—	—	GHz	
t_{PD}	Propagation Delay(2)	220	300	380	220	300	380	220	300	380	ps	
t_{SKEW}(3)	Within-Device Skew	—	20	25	—	20	25	—	20	25	ps	
	Part-to-Part Skew(4)	—	85	160	—	85	160	—	85	160	ps	
t_{JITTER}	Cycle-to-Cycle Jitter (rms)	—	0.2	< 1	—	0.2	< 1	—	0.2	< 1	ps_{RMS}	
V_{PP}	Minimum Input Swing(5)	150	800	1200	150	800	1200	150	800	1200	mV	
t_r, t_r	Output Rise/Fall Times (20% to 80%)	100	150	250	100	150	250	100	150	250	ps	

Note 1. f_{MAX} guaranteed for functionality only (toggel frequency).

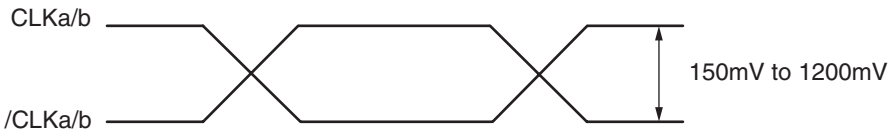
Note 2. CLK 0 to Bank A and CLK 1 to Bank B; Differential. Maximum propagation delay is worst-case, over temperature and voltage.

Note 3. Skew is measured between outputs under identical transitions.

Note 4. Measured for same transitions.

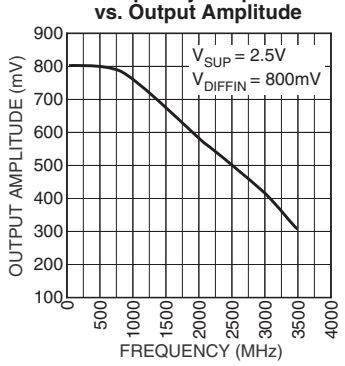
Note 5. See “Timing Waveform.”

TIMING WAVEFORM

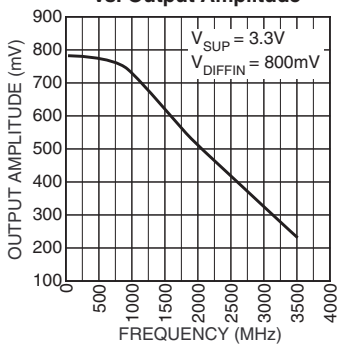


TYPICAL CHARACTERISTICS

Frequency Response vs. Output Amplitude



Frequency Response vs. Output Amplitude



TERMINATION RECOMMENDATIONS

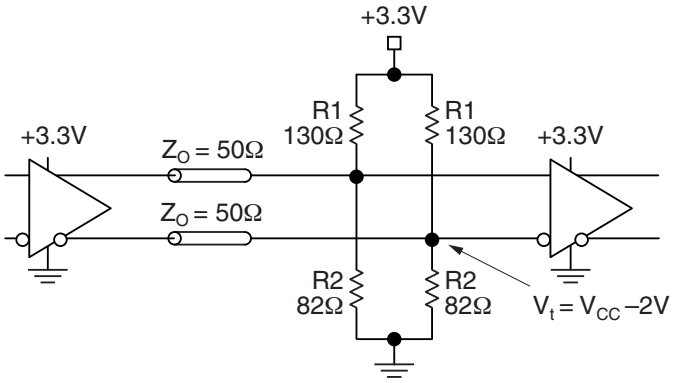


Figure 1. Parallel Termination–Thevenin Equivalent

Note 1. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω.

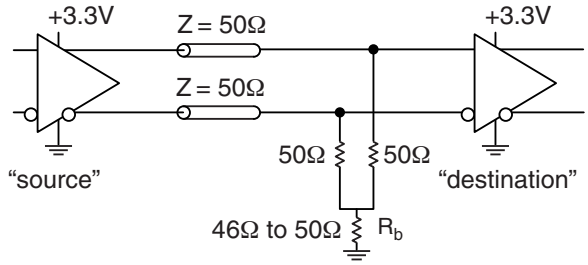


Figure 2. Three-Resistor "Y–Termination"

Note 1. Power-saving alternative, Thevenin termination.

Note 2. Place termination resistors as close to destination inputs as possible.

Note 3. R_b resistor sets the DC bias voltage, equal to V_t.

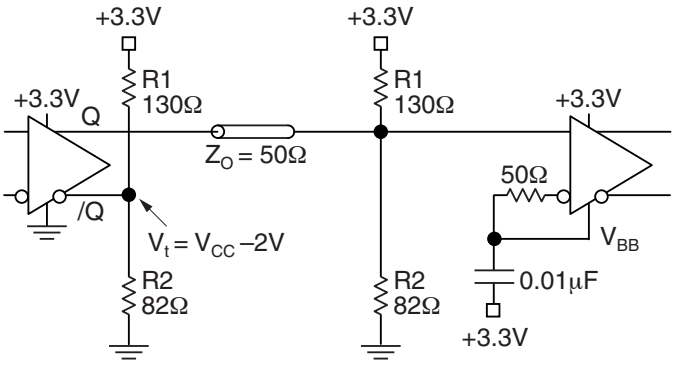


Figure 3. Terminating Unused I/O

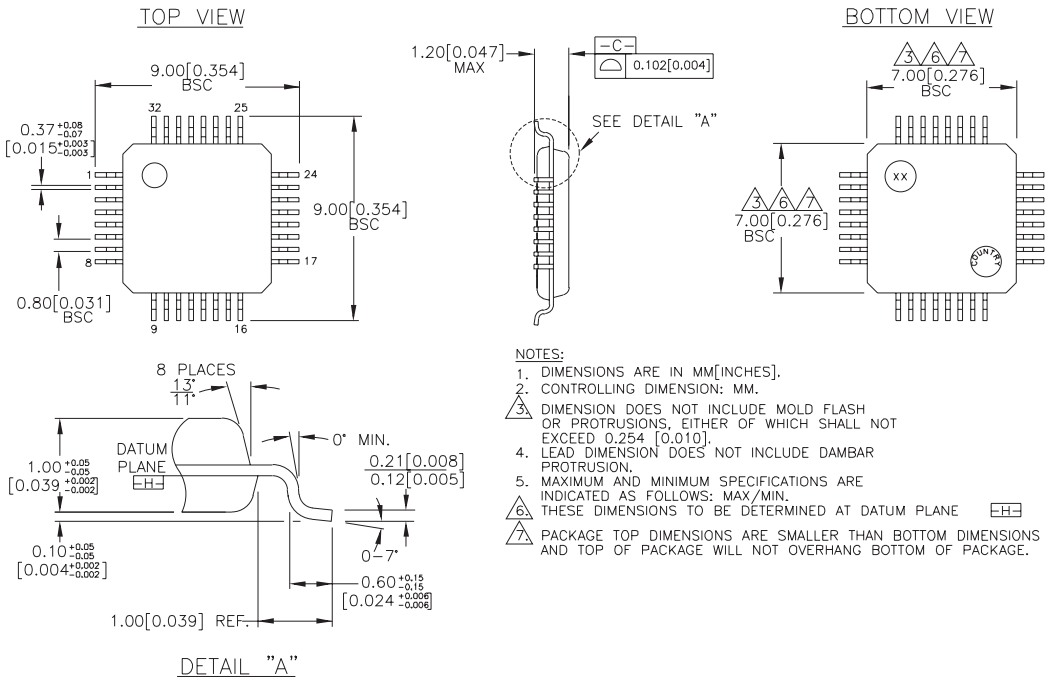
Note 1. Unused output (/Q) must be terminated to balance the output.

Note 2. Micrel's differential I/O logic devices include a V_{BB} reference pin .

Note 3. Connect unused input through 50Ω to V_{BB}. Bypass with a 0.01μF capacitor to GND.

Note 4. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω.

32-PIN THIN QUAD FLATPACK (T32-1)



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.

Rev. 01

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