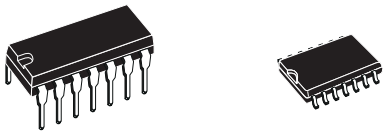
HCF4541B

PROGRAMMABLE TIMER

- 16 STAGE BINARY COUNTER
- LOW SYMMETR. OUTPUT RESISTANCE, TYPICALLY 100Ω at V_{DD} = 15V
- OSCILLATOR FREQUENCY RANGE : DC to 100KHz
- AUTO OR MASTER RESET DISABLES OSCILLATOR DURING RESET TO REDUCE POWER DISSIPATION
- OPERATES WITH VERY SLOW CLOCK RISE AND FALL TIMES
- BUILT-IN LOW-POWER RC OSCILLATOR
- EXTERNAL CLOCK (applied to pin 3) CAN BE USED INSTEAD OF OSCILLATOR
- OPERATES AS 2^n FREQUENCY DIVIDER OR AS A SINGLE-TRANSITION TIMER
- Q/$\overline{Q}$ SELECT PROVIDES OUTPUT LOGIC LEVEL FLEXIBILITY
- CAPABLE OF DRIVING SIX LOW POWER TTL LOADS, THREE LOW POWER SCHOTTKY LOADS, OR SIX HTL LOADS OVER THE RATED TEMP. RANGE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- 100% TESTED FOR QUIESCENT CURRENT AT 20V
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP SOP

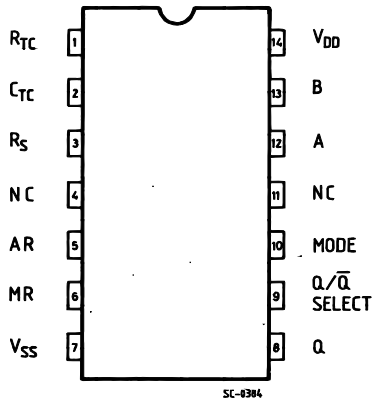
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4541BEY	
SOP	HCF4541BM1	HCF4541M013TR

DESCRIPTION

The HCF4541B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
This device is composed of a 16-stages binary counter, an oscillator controlled by 2 external resistors and a capacitor, an output control logic and an automatic power-on reset circuit. The counter varies on positive-edge clock transition and it can be cleared by the MASTER RESET input. The output from this timer is the Q or $\overline{Q}$ output from the 8th, 13th, or 16th counter stage. The choice of the stage depends on the time

PIN CONNECTION

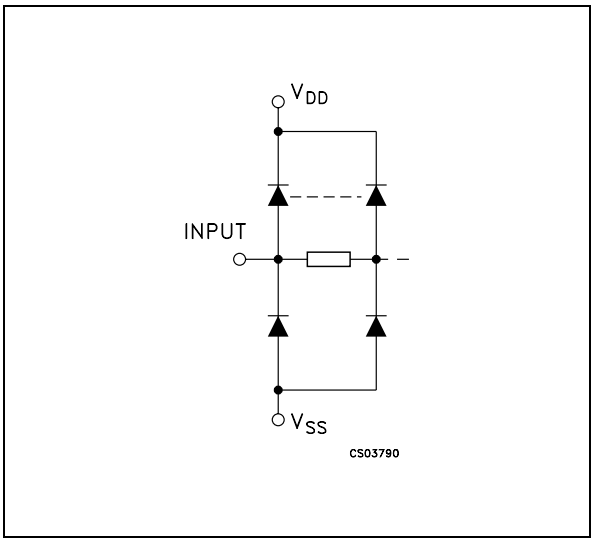


select inputs A or B (see frequency selection table). The output is available in one of the two modes that can be selected via the MODE input pin 10 (see truth table). The output turns out as a continuos square wave, with a frequency equal to the oscillator frequency divided by 2^N when this MODE input is a logic "1". When it is a logic "0" and after a MASTER RESET is started, and Q output has been selected, the output goes up to a high state after 2^{N-1} counts. It remains in that state till another MASTER RESET pulse is apply or the mode input is a logic "1". The process starts by setting the AUTO RESET input (pin 5) to logic "0" and switching power on. If pin 5 is set to logic "1", the AUTO RESET circuit is not enabled and counting cannot start till a positive MASTER RESET pulse is applied, returning to a low level. The AUTO RESET consumes a remarkable amount of power and should not be used if low power operation is wanted. The frequency of the oscillator depends on the RC network. It can be calculated using the following formula :

$f = 1 / 2.3\ R_{TC}\ C_{TC}$

where f is between 1KHz and 100KHz and RS $\geq$ 10 KΩ and $\approx 2\ R_{TC}$

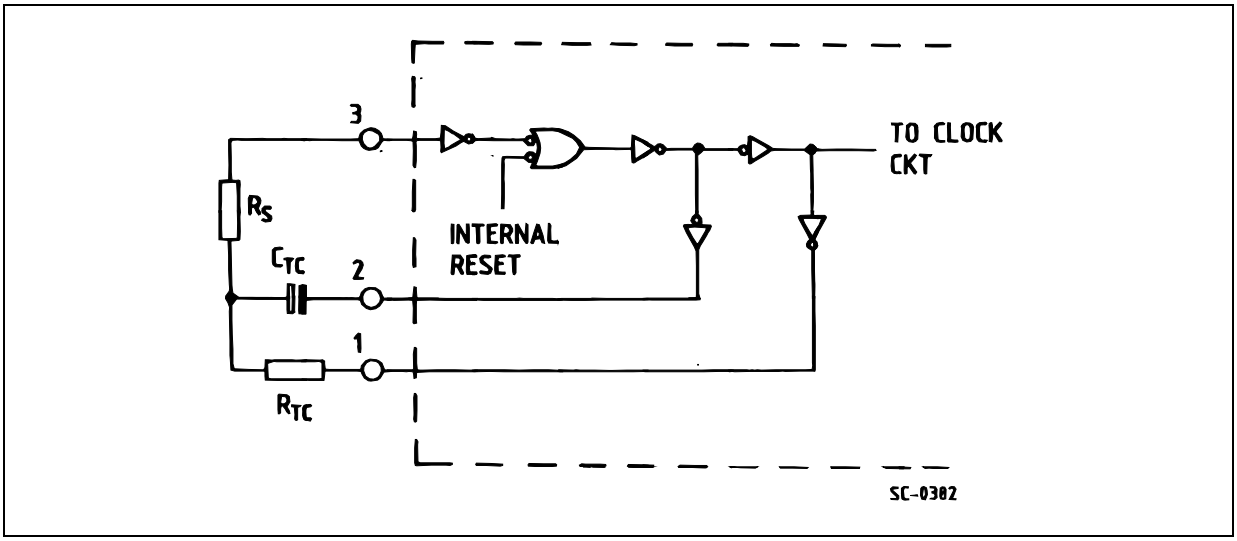
INPUT EQUIVALENT CIRCUIT



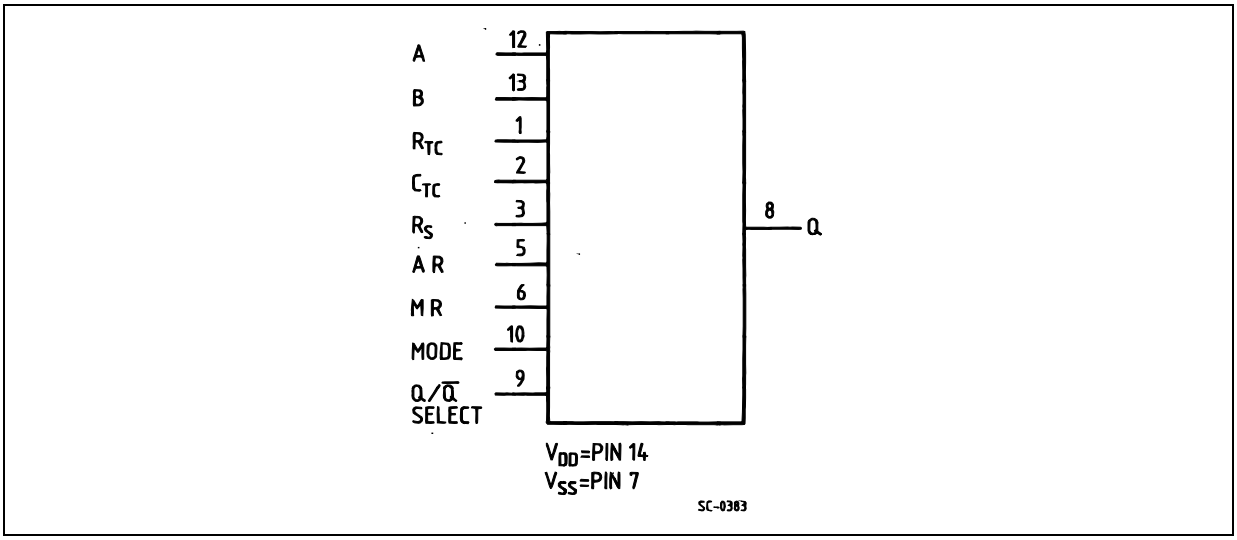
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
12, 13	A, B	Time Select Input
4, 11	NC	Not Connected
1, 2	R_{TC}, C_{TC}	External Resistor, Capacitor Connection
3	R_S	External Resistor Connection or External Clock Input
5	AR	Auto Reset Input
6	MR	Master Reset Input
10	MODE	Mode Select Input
9	Q/$\overline{Q}$ SELECT	Output Selector
8	Q	Output
7	V_{SS}	Negative Supply Voltage
14	V_{DD}	Positive Supply Voltage

RC OSCILLATOR CIRCUIT



FUNCTIONAL DIAGRAM



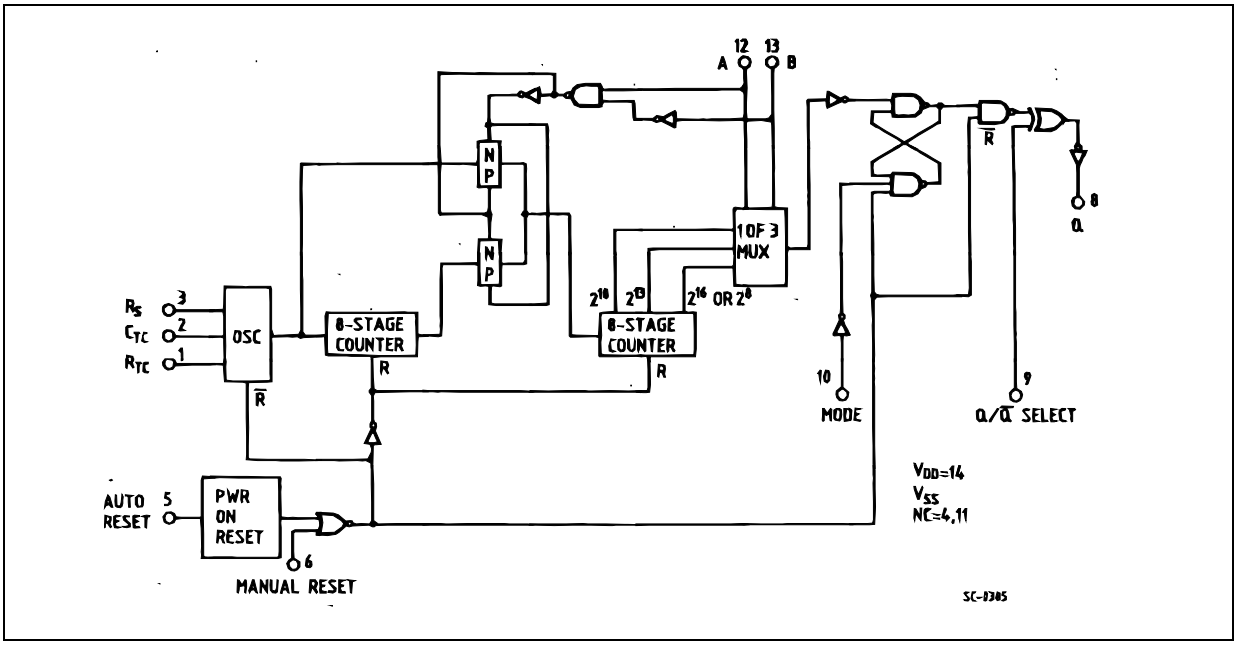
FREQUENCY SELECTION TABLE

A	B	N. of Stages N	Count 2^N
L	L	13	8192
L	H	10	1024
H	L	8	256
H	H	16	65536

TRUTH TABLE

PIN	STATE	
	L	H
5	Auto Reset On	Auto Reset Disable
6	Master Reset Off	Master Reset On
9	Output Initially Low After Reset (Q)	Output Initially High After Reset ($\overline{Q}$)
10	Single Transition Mode	Recycle Mode

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.55	-3.1		-1.08		-1.08		mA
		0/5	4.6	<1	5	-5	-10		-3		-4.1		
		0/10	9.5	<1	10	-4	-8		-3.3		-3.3		
		0/15	13.5	<1	15	-10	-20		-8.4		-8.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	1.55	3.1		1.08		1.08		mA
		0/10	0.5	<1	10	4	8		3.3		3.3		
		0/15	1.5	<1	15	10	20		8.4		8.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

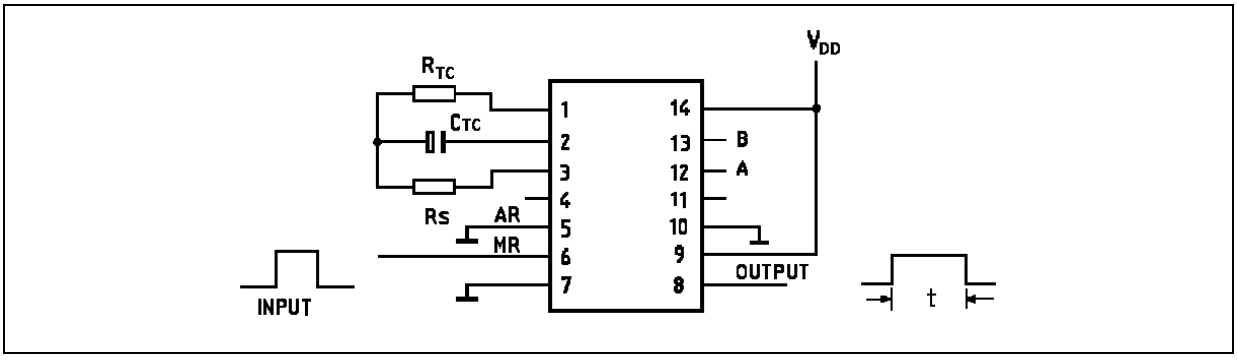
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
(2^8) t_{PHL} t_{PLH}	Propagation Delay Time (CLOCK to Q)	5			3.5	10.5	µs
		10			1.25	3.8	
		15			0.9	2.9	
(2^{16}) t_{PHL} t_{PLH}	Propagation Delay Time (CLOCK to Q)	5			6	18	µs
		10			3.5	10	
		15			2.5	7.5	
t_{THL}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_{TLH}	Transition Time	5			180	360	ns
		10			90	180	
		15			65	130	
	Master Reset, Clock Pulse Width	5		900	300		ns
		10		300	100		
		15		225	85		
f_{CL}	Maximum Clock Pulse Input Frequency	5			1.5		MHz
		10			4		
		15			6		
t_r, t_f	Maximum Clock Pulse Input Rise or Fall Time	5		Unlimited			µs
		10					
		15					

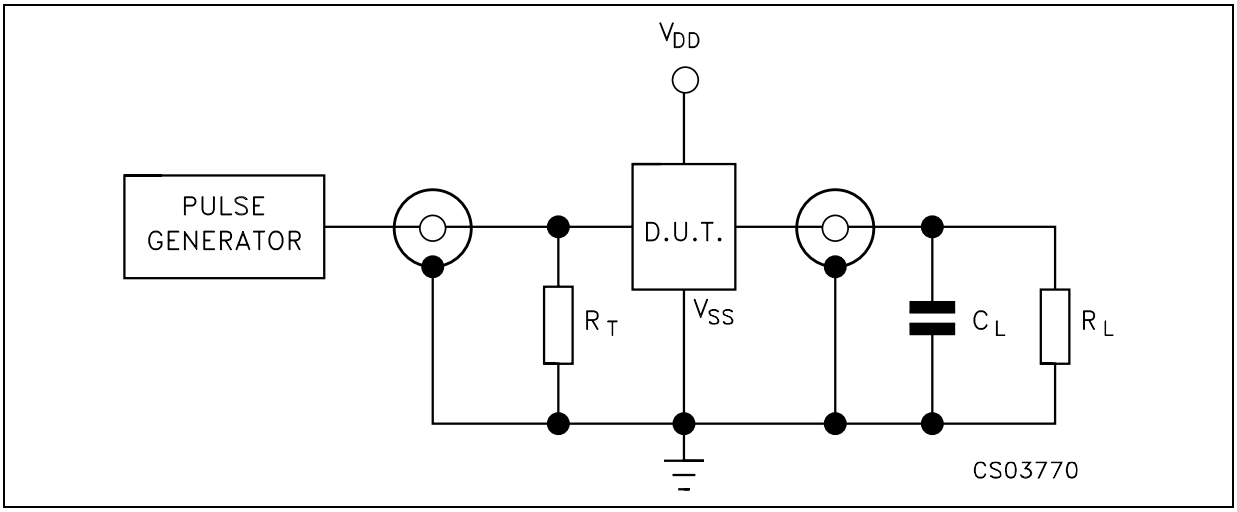
(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

DIGITAL TIMER APPLICATION



A positive MASTER RESET pulse clears the counter and latch. The Output goes high and keeps up till the number of pulses, selected by A and B , are counted. This circuit is retriggerable and is as accurate as the input frequency. If a more accurate circuit is desired, an external clock can be used on pin 3. A set-up time equal to the width of the one shot output is required immediately following initial power up, during which time the output will be high

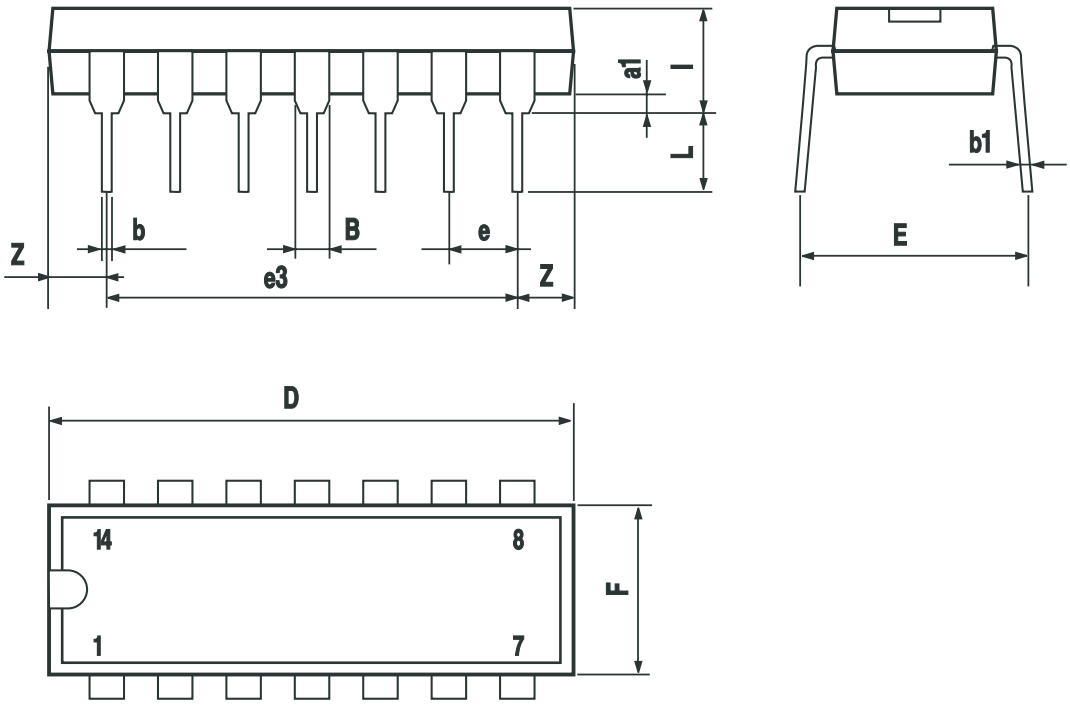
TEST CIRCUIT



C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Plastic DIP-14 MECHANICAL DATA

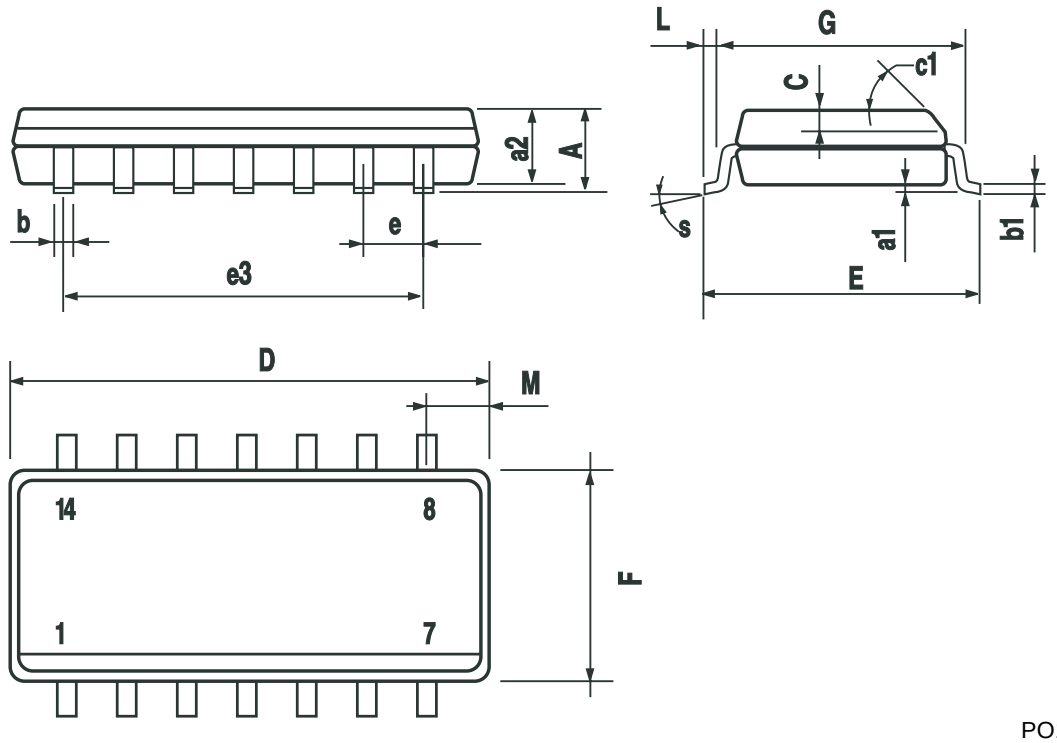
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



P001A

SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



PO13G