19-0479; Rev 1; 7/97

EVALUATION KIT AVAILABLE

622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

General Description

The MAX3664 low-power transimpedance preamplifier for 622Mbps SDH/SONET applications consumes only 85mW. Operating from a single +3.3V supply, it converts a small photodiode current to a measurable differential voltage. A DC cancellation circuit provides a true differential output swing over a wide range of input current levels, thus reducing pulse-width distortion. The differential outputs are back-terminated with 60Ω per side.

The transimpedance gain is nominally 6kΩ. For input signal levels beyond approximately 100µAp-p, the amplifier will limit the output swing to 900mV. The MAX3664's low 55nA input noise provides a typical sensitivity of -33.2dBm in 1300nm, 622Mbps receivers.

The MAX3664 is designed to be used in conjunction with the MAX3675 clock recovery and data retiming IC with limiting amplifier. Together, they form a complete 3.3V, 622Mbps SDH/SONET receiver.

In die form, the MAX3664 is designed to fit on a header with a PIN diode. It includes a filter connection, which provides positive bias for the photodiode through a 1kΩ resistor to V_{CC}. The device is also available in 8-pin SO and µMAX packages.

Applications

SDH/SONET Receivers

PIN/Preamplifier Receivers

Regenerators for SDH/SONET

Features

- **Single +3.3V Supply Operation**
- **55nA$_{RMS}$ Input-Referred Noise**
- **6kΩ Gain**
- **85mW Power**
- **300µA Peak Input Current**
- **200ps Max Pulse-Width Distortion**
- **Differential Output Drives 100Ω Load**
- **590MHz Bandwidth**

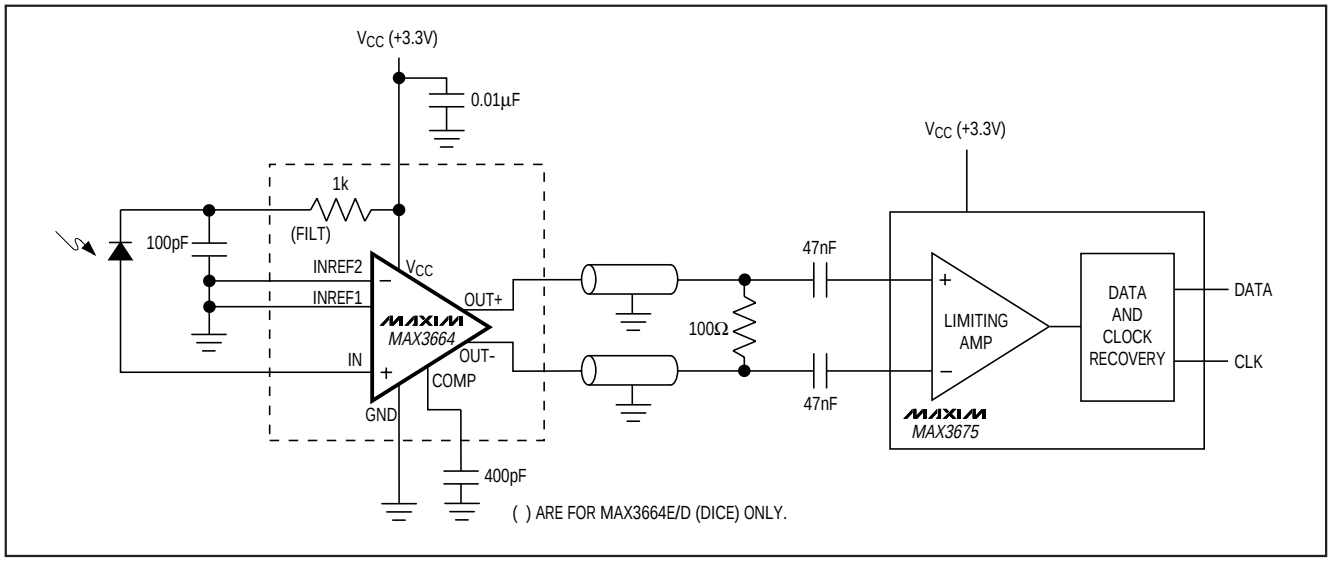
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3664E/D	-40°C to +85°C	Dice
MAX3664ESA	-40°C to +85°C	8 SO
MAX3664EUA*	-40°C to +85°C	8 µMAX

** Contact factory for package availability.*

Pin Configuration appears at end of data sheet.

Typical Application Circuit



622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

ABSOLUTE MAXIMUM RATINGS

V_{CC} .....-0.5V to +5.5V
Continuous Current
IN, INREF1, INREF2, COMP, FILT.....5mA
OUT+, OUT-.....25mA
Continuous Power Dissipation (T_A = +85°C)
SO (derate 5.88mW/°C above +85°C).....383mW
µMAX (derate 4.1mW/°C above +85°C) 268mW
Operating Junction Temperature (die).....-40°C to +150°C
Processing Temperature (die) .....+400°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V ±0.3V, COMP = GND, 100Ω load between OUT+ and OUT-, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Voltage	V_{IN}	I_{IN} = 0 to 300µA		0.8	0.95	V
Gain Nonlinearity		I_{IN} = 0 to 20µA			±5	%
Supply Current	I_{CC}	I_{IN} = 0	12	25	35	mA
Small-Signal Transimpedance	z_{21}	Differential output	4.5	6	7.5	kΩ
Output Common-Mode Level				V_{CC} - 1.3		V
Power-Supply Rejection Ratio	PSRR	f < 1MHz, referred to output	20			dB
Differential Output Offset	ΔV_{OUT}	I_{IN} = 200µA, C_{COMP} = 400pF		±7		mV
Output Impedance (per side)	Z_{OUT}		40	60	75	Ω
Maximum Output Voltage	V_{OUT}(max)	I_{IN} = 300µA			950	mV
Filter Resistor (die only)	R_{FILT}		800	1000	1200	Ω

Note 1: Dice are tested at T_j = +27°C.
Note 2: µMAX package tested at T_A = +25°C to +85°C.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V ±0.3V, C_{COMP} = 400pF, C_{IN} = 1.1pF, outputs terminated into 50Ω, 8-pin SO package in MAX3664 EV board, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

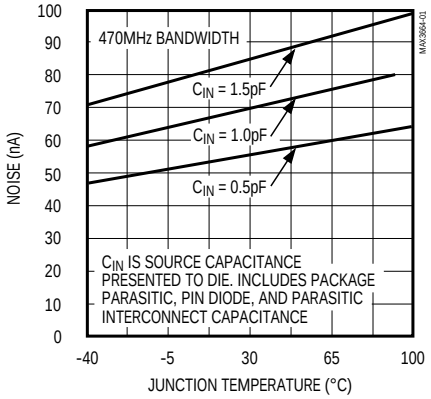
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Bandwidth	BW_{-3dB}	Relative to gain at 10MHz		590		MHz
Low-Frequency Cutoff					150	kHz
Pulse-Width Distortion (Note 5)	PWD	2µA to 100µA peak input current, 50% duty cycle, 1–0 pattern		6	100	ps
		100µA to 300µA peak input current, 50% duty cycle, 1–0 pattern		80	200	
RMS Noise Referred to Input	i_n	C_{IN} = 0.3pF (Note 6), I_{IN} = 0		55		nA
		C_{IN} = 1.1pF (Note 6), I_{IN} = 0		73	86	

Note 3: AC Characteristics are guaranteed by design.
Note 4: C_{IN} is the total capacitance at IN.
Note 5: $PWD = \left| \frac{2 \times \text{Pulse width} - \text{Period}}{2} \right|$
Note 6: DC to 470MHz, measured with 3-pole Bessel filter at output.

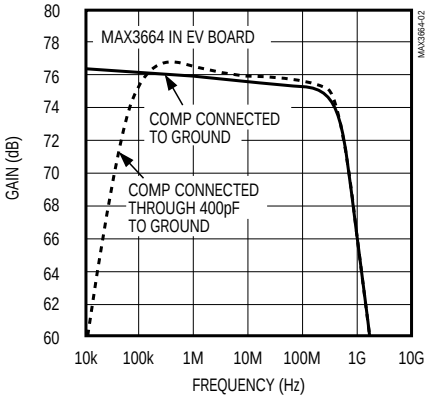
Typical Operating Characteristics

(V_{CC} = +3.3V, C_{COMP} = 400pF, T_A = +25°C, unless otherwise noted.)

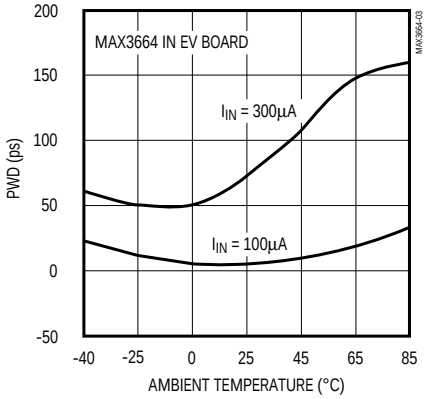
INPUT-REFERRED NOISE vs. TEMPERATURE



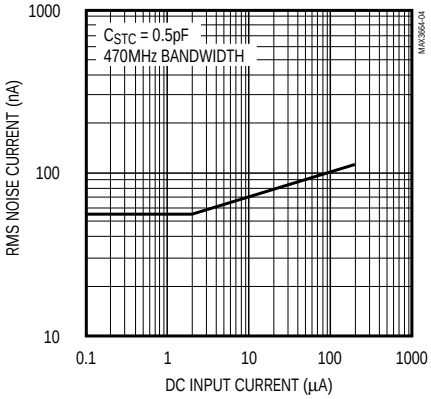
SMALL-SIGNAL GAIN vs. FREQUENCY



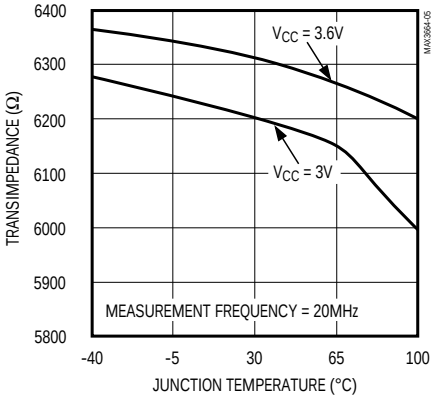
PULSE-WIDTH DISTORTION vs. TEMPERATURE



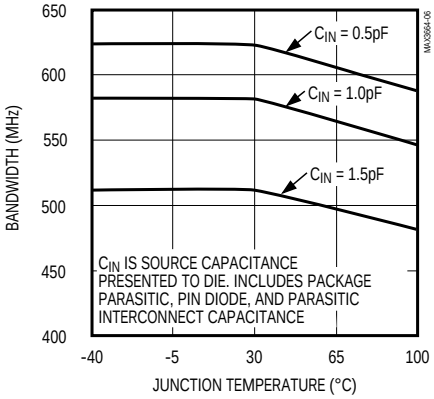
INPUT-REFERRED RMS NOISE CURRENT vs. DC INPUT CURRENT



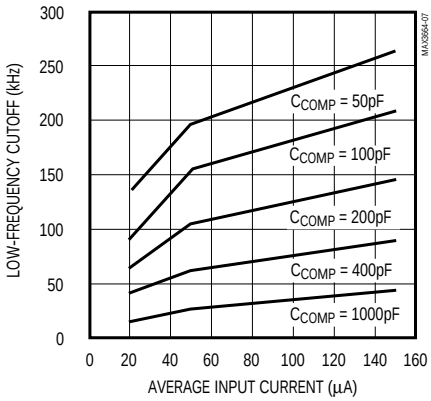
SMALL-SIGNAL TRANSIMPEDANCE vs. TEMPERATURE



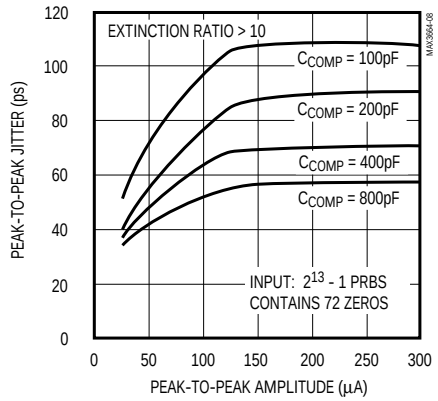
BANDWIDTH vs. TEMPERATURE



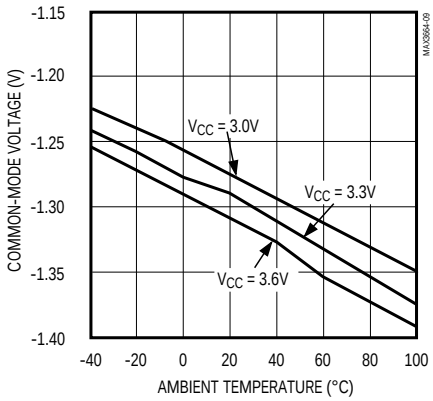
LOW-FREQUENCY CUTOFF vs. AVERAGE INPUT CURRENT



DATA-DEPENDENT JITTER vs. INPUT SIGNAL AMPLITUDE



OUTPUT COMMON-MODE VOLTAGE (REFERENCED TO V_{CC}) vs. TEMPERATURE

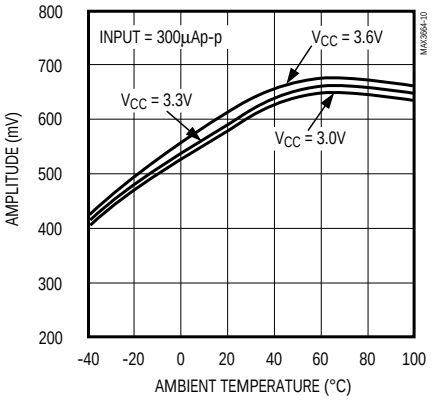


622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

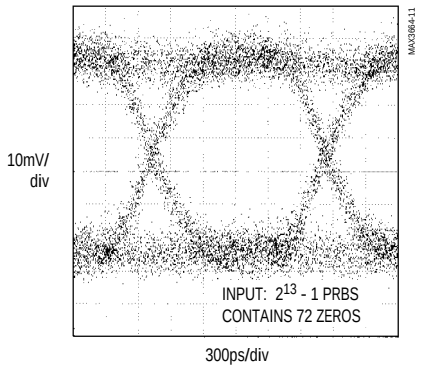
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, C_{COMP} = 400pF, T_A = +25°C, unless otherwise noted.)

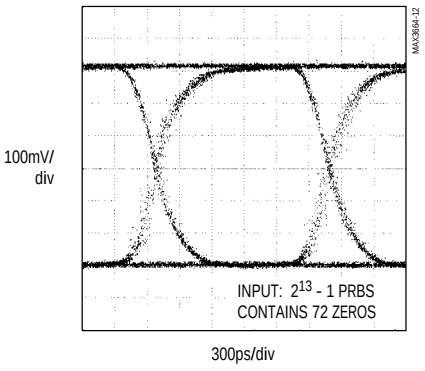
OUTPUT AMPLITUDE vs. TEMPERATURE



EYE DIAGRAM (INPUT = 10µAp-p)



EYE DIAGRAM (INPUT = 300µAp-p)



Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	+3.3V Supply Voltage
2	IN	Signal Input
3, 4	INREF1, INREF2	Input References 1 and 2. Connect to photodetector AC ground.
5	GND	Ground
6	OUT+	Noninverting Voltage Output. Current flowing into IN causes V_{OUT+} to increase.
7	OUT-	Inverting Voltage Output. Current flowing into IN causes V_{OUT-} to decrease.
8	COMP	External Compensation Capacitor for DC cancellation loop. Connect 400pF or more from COMP to GND for normal operation. Connect COMP directly to GND to disable the DC cancellation loop.
—	FILT*	Filter Connection. Provides positive bias for photodiode through a 1kΩ resistor to V_{CC}. See *Step 3: Designing Filters*. (This pad is accessible on the die only.)

** MAX3664E/D (die) only.*

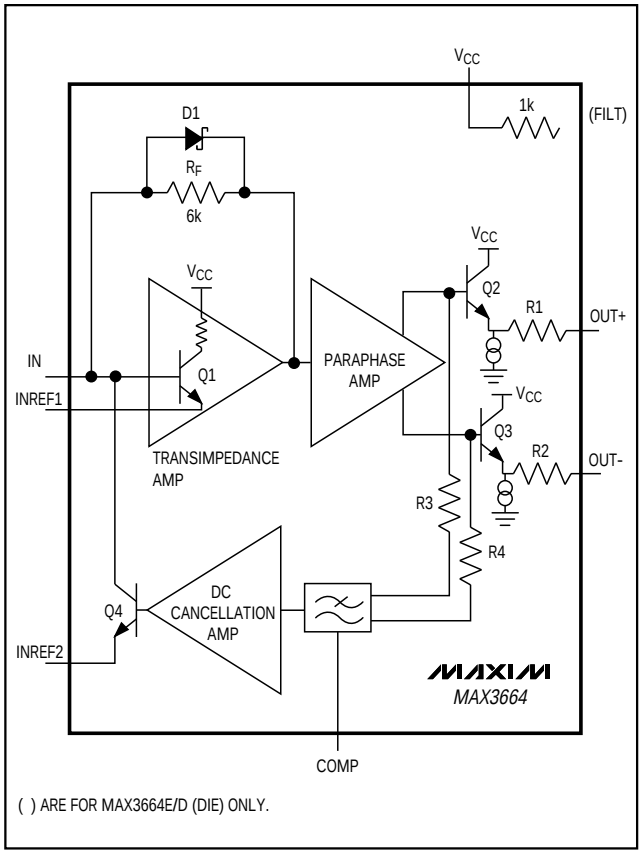


Figure 1. Functional Diagram

Detailed Description

The MAX3664 is a transimpedance amplifier designed for 622Mbps SDH/SONET applications. It comprises a transimpedance amplifier, a paraphase amplifier with emitter-follower outputs, and a DC cancellation loop. Figure 1 is a functional diagram of the MAX3664.

Transimpedance Amplifier

The signal current at IN flows into the summing node of a high-gain amplifier. Shunt feedback through R_F converts this current to a voltage with a gain of 6kΩ. Diode D1 clamps the output voltage for large input currents. INREF1 is a direct connection to the emitter of the input transistor, and must be connected directly to the photodetector AC ground return for best performance.

Paraphase Amplifier

The paraphase amplifier converts single-ended inputs to differential outputs, and introduces a voltage gain of 2. This signal drives a pair of internally biased emitter followers, Q2 and Q3, which form the output stage. Resistors R1 and R2 provide back-termination at the output, absorbing reflections between the MAX3664 and its load.

The output emitter followers are designed to drive a 100Ω differential load between OUT+ and OUT-. They can also drive higher output impedances, resulting in increased gain and output voltage swing.

DC Cancellation Loop

The DC cancellation loop removes the DC component of the input signal by using low-frequency feedback. This feature centers the signal within the MAX3664's dynamic range, reducing pulse-width distortion on large input signals.

The output of the paraphase amplifier is sensed through resistors R3 and R4 and then filtered, amplified, and fed back to the base of transistor Q4. The transistor draws the DC component of the input signal away from the transimpedance amplifier's summing node.

The COMP pin sets the DC cancellation loop's response. Connect 400pF or more between COMP and GND for normal operation. Connect the pin directly to GND to disable the loop. The DC cancellation loop can sink up to 300µA of current at the input. When operated with C_{COMP} = 400pF, the loop takes approximately 20µs to stabilize.

The MAX3664 minimizes pulse-width distortion for data sequences that exhibit a 50% duty cycle. A duty cycle other than 50% causes the device to generate pulse-width distortion.

DC cancellation current is drawn from the input and adds noise. For low-level signals with little or no DC component, this is not a problem. Preamplifier noise will increase for signals with significant DC component.

Applications Information

The MAX3664 is a low-noise, wide-bandwidth transimpedance amplifier that is ideal for 622Mbps SDH/SONET receivers. Its features allow easy design into a fiber optic module, in four simple steps.

Step 1: Selecting a Preamplifier for a 622Mbps Receiver

Fiber optic systems place requirements on the bandwidth, gain, and noise of the transimpedance preamplifier. The MAX3664 optimizes these characteristics for SDH/SONET receiver applications that operate at 622Mbps.

In general, the bandwidth of a fiber optic preamplifier should be 0.6 to 1 times the data rate. Therefore, in a 622Mbps system, the bandwidth should be between 375MHz and 622MHz. Lower bandwidth causes pattern-dependent jitter and a lower signal-to-noise ratio, while higher bandwidth increases thermal noise. The MAX3664 typical bandwidth is 590MHz, making it ideal for 622Mbps applications.

The preamplifier's transimpedance must be high enough to ensure that expected input signals generate output levels exceeding the sensitivity of the limiting amplifier (quantizer) in the following stage. The MAX3675 clock recovery and limiting amplifier IC has an input sensitivity of 3.6mVp-p, which means that 3.6mVp-p is the minimum signal amplitude required to produce a fully limited output. Therefore, when used with the MAX3664, which has a 6kΩ transimpedance, the minimum detectable photodetector current is 600nA.

It is common to relate peak-to-peak input signals to average optical power. The relationship between optical input power and output current for a photodetector is called the responsivity (ρ), with units Amperes/Watt (A/W). The photodetector peak-to-peak current is related to the peak-to-peak optical power as follows:

$$Ip\text{-}p = (Pp\text{-}p)(\rho)$$

Based on the assumption that SDH/SONET signals maintain a 50% duty cycle, the following equations relate peak-to-peak optical power to average optical power and extinction ratio (Figure 2):

Average Optical Power = $P_{AVE} = (P0 + P1) / 2$

Extinction Ratio = $r_e = P1 / P0$

Peak-to-Peak Signal Amplitude = $Pp\text{-}p = P1 - P0$

Therefore,

$$P_{AVE} = Pp\text{-}p\ (1 / 2)[(r_e + 1) / (r_e - 1)]$$

622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

In a system where the photodiode responsivity is 0.9A/W and the extinction ratio is 10, the MAX3664/MAX3675 receiver with 670nA gain sensitivity will deliver a fully limited output for signals of average optical power larger than:

(600nA / 0.9A/W)(1 / 2)(11 / 9) = 407nW ⇒ -33.9dBm

Sensitivity is a key specification of the receiver module. The ITU/Bellcore specifications for SDH/SONET receivers require a link sensitivity of -27dBm with a bit error rate (BER) of 1E - 10. There is an additional 1dB power penalty to accommodate various system losses; therefore, the sensitivity of a 622Mbps receiver must be better than -28dBm.

Although several parameters affect sensitivity (such as the quantizer sensitivity and preamplifier gain, as previously discussed), most fiber optic receivers are designed so that noise is the dominant factor. Noise from the high-gain transimpedance amplifier, in particular, determines the sensitivity. The noise generated by the MAX3664 can be modeled with a Gaussian distribution. In this case, a BER of 1E - 10 corresponds to a peak-to-peak signal amplitude to RMS noise ratio (SNR) of 12.7. The MAX3664's typical input-referred noise, i_n, (bandwidth-limited to 470MHz) is $55nA_{RMS}$. Therefore, the minimum input for a BER of 1E - 10 is (12.7 x 55nA) = 700nAp-p. Rearranging the previous equations in these terms results in the following relation:

Optical Sensitivity (dBm) =
$-10\log[(i_n / \rho)(SNR)(1/2)(r_e + 1) / (r_e - 1)(1000)]$

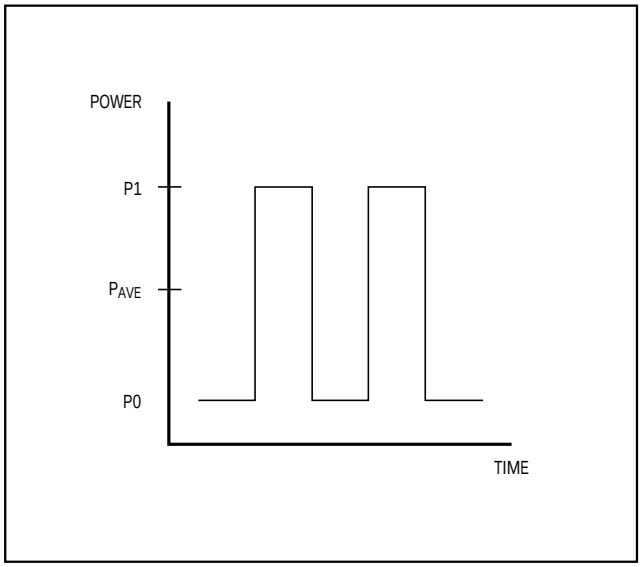


Figure 2. Optical Power Definitions

At room temperature, with r_e = 10, SNR = 12.7, i_n = 55nA, and ρ = 0.9A/W, the MAX3664 sensitivity is -33.2dBm. At +85°C, noise increases to 62nA and sensitivity decreases to -32.7dBm. The MAX3664 provides 4.7dB margin over the SDH/SONET specifications, even at +85°C.

The largest allowable input to an optical receiver is called the input overload. The MAX3664's largest input current (I_{max}) is 300µAp-p, with 200ps of pulse-width distortion. The pulse-width distortion and input current are closely related (see *Typical Operating Characteristics*). If the clock recovery circuit can accept more pulse-width distortion, a higher input current might be acceptable. For worst-case responsivity and extinction ratio, ρ = 1A/W and $r_e = \infty$, the input overload is:

Overload (dBm) = $-10\log (I_{max})(1 / 2)(1000)$

For I_{max} = 300µA, the MAX3664 overload is -8.2dBm.

Step 2: Selecting Time Constants

A receiver built with the MAX3664 will have a bandpass frequency response. The low-frequency cutoff causes unwanted data-dependent jitter and sensitivity loss. Because SDH/SONET data streams contain scrambled data, certain data sequences may generate continuous successions of 1s or 0s. The low-frequency cutoff forces the output of such sequences to zero, ultimately causing a sensitivity reduction. The SDH specifications state that a receiver must be able to handle up to 72 consecutive bits of the same value within the data. Therefore, choose the low-frequency cutoff to ensure an acceptable amount of data-dependent jitter and sensitivity loss.

Determine the reduction in signal-to-noise ratio due to a transitionless sequence of duration t as follows:

$$SNR_{loss} = 1 - e^{-t / \tau} = 1 - e^{-(2\pi f_C t)}$$

where τ is the time constant of the offset correction, f_C is the low-frequency cutoff, and t is the time for 72 bits (116ns for a 622Mbps data rate).

Suppose that the receiver should not have more than 0.25dB (6%) of sensitivity loss due to a 72-bit transitionless sequence. This means that:

$$(1 - e^{-(2\pi f_C)(116ns)}) < 0.06$$

$$f_C = (\ln 0.94) / [(-2\pi)(116ns)] = 85kHz \text{ (max)}$$

The loss of sensitivity is a concern only when the SNR is small (close to 12.7), which occurs with input currents less than 3µAp-p.

The cutoff frequency also affects the data-dependent jitter (DDJ). DDJ due to low-frequency cutoff can be approximated as droop / slope, where the slope in V/sec is measured at the 50% crossing of an eye diagram, and droop is the loss-of-signal to noise calculated above as $1 - e^{-(2\pi f_c t)}$. The slope at the 50% crossing is typically two times the 10% to 90% slope, which is approximately 0.35 / bandwidth. For a 622Mbps receiver with a 470MHz bandwidth, the 10% to 90% rise time is approximately 750ps. The slope through the 50% crossing will be approximately:

Amplitude (2)(0.8) / 750ps =
1.6 Amplitude / 750ps = 2E9 Amplitude V/sec

$DDJ = 2\,[\text{Amplitude}\,(1 - e^{-(2\pi f_c t)})]\,/$
$[\ 2.0E9\ \text{Amplitude}\ ] = (1 - e^{-(2\pi f_c t)})\,/\,(1E9)$

OR

$f_c = -\ln[1 - (1.0E9)(DDJ)]\,/\,[2\pi t]$

If the maximum allowable DDJ is 100ps, and t = 112ns for a 72-bit sequence, then the maximum low-frequency cutoff is 150kHz.

Several circuits in the receiver can determine the low-frequency cutoff. In a receiver using the MAX3664 and MAX3675, there are three locations for concern:

1) The MAX3664's DC cancellation circuit.
2) The coupling capacitors between the MAX3664 outputs and MAX3675 inputs.
3) The MAX3675's offset correction circuit.

The highest cutoff frequency in the system determines the amount of data-dependent jitter created.

The time constants of the MAX3675's offset correction and of the coupling capacitors should be separated by a factor of ten (one decade) to prevent low-frequency oscillations.

For example, select the offset correction of the MAX3664 to set the receiver cutoff frequency. Note that the MAX3664's low-frequency cutoff increases with average input current. Since DDJ increases with f_C, it follows that DDJ increases as average input increases. When the input signal is large enough to limit the outputs, however, DDJ does not increase. Therefore, the maximum DDJ results from the lowest input that causes the MAX3664 to have limited outputs (see *Typical Operating Characteristics*), which is about 150µAp-p. When selecting a capacitor for the COMP pin that achieves your desired DDJ, use the data from *Typical Operating Characteristics* at I_{INPUT} = 150µA.

In summary, use the following method to select the low-frequency cutoff that will provide the sensitivity and DDJ required for SDH/SONET receivers:

1) Determine the longest time without transitions.
2) Determine the acceptable loss of SNR ratio, and the acceptable DDJ due to the transitionless time.
3) Estimate the low-frequency cutoff required for either the worst-case SNR loss or for DDJ.
4) Select the location in the receiver to determine the highest cutoff frequency. Normally, the MAX3664 would determine the dominant low-frequency cutoff. Then select all other low-frequency cutoffs one decade lower.
5) Select a capacitor for the COMP pin from the *Typical Operating Characteristics* graphs. 400pF is adequate for most 622Mbps SDH/SONET applications.

622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

Step 3: Designing Filters

The MAX3664's noise performance is a strong function of the circuit's bandwidth, which changes over temperature and varies from lot to lot. The receiver sensitivity can be improved by adding filters to limit this bandwidth. Filter designs can range from a one-pole filter using a single capacitor, to more complex filters using inductors. Figure 3 illustrates two examples: the simple filter provides moderate roll-off with minimal components, while the complex filter provides a sharper roll-off and better transient response.

Supply voltage noise at the cathode of the photodiode produces a current $I = C_{PHOTO} (\Delta V/\Delta t)$, which reduces the receiver sensitivity. C_{PHOTO} is the photodiode capacitance.

The FILT resistor of the MAX3664, combined with an external capacitor (see *Typical Operating Circuit*) can be used to reduce this noise. The external capacitor (C_{FILT}) is placed in parallel with the photodiode. Current generated by supply noise is divided between C_{FILT} and C_{PHOTO}. The input noise current due to supply noise is (assuming the filter capacitor is much larger than the photodiode capacitance):

$$I_{NOISE} = \frac{(V_{NOISE})(C_{PHOTO})}{(R_{FILT})(C_{FILTER})}$$

If the amount of tolerable noise is known, then the filter capacitor can be easily selected:

$$C_{FILT} = \frac{(V_{NOISE})(C_{PHOTO})}{(R_{FILT})(I_{NOISE})}$$

For example, with maximum noise voltage = 100mVp-p, C_{PHOTO} = 0.5pF, R_{FILT} = 1kΩ, and I_{NOISE} selected to be 5nA (1/10 of MAX3664 input-referred noise):

$$C_{FILT} = (0.1)(0.5E-12)/[(1000)(5E-9)] = 10nF$$

Step 4: Designing a Low-Capacitance Input

Noise performance and bandwidth are adversely affected by stray capacitance on the input node. Select a low-capacitance photodiode and use good high-frequency design and layout techniques to minimize capacitance on this pin. The MAX3664 is optimized for 0.5pF of capacitance on the input—approximately the capacitance of a photodetector diode sharing a common header with the MAX3664 in die form.

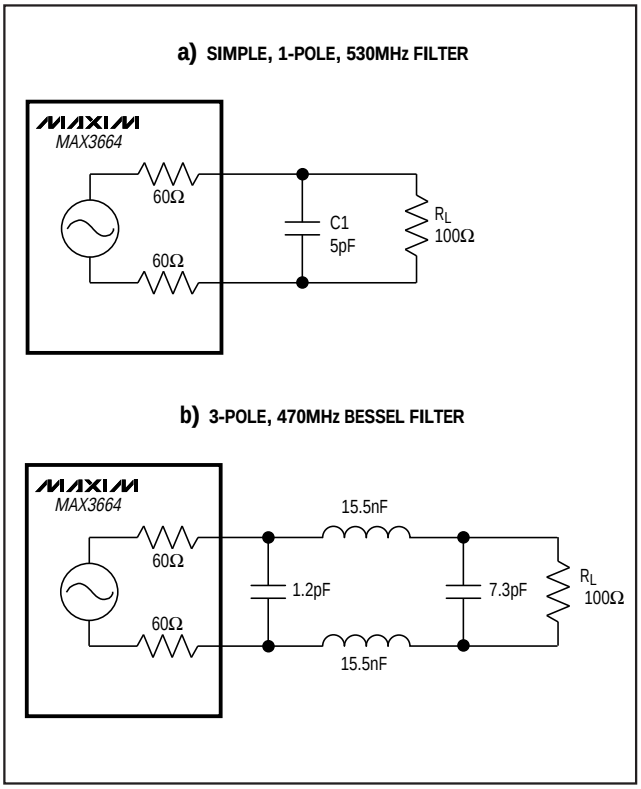


Figure 3. Filter Design Examples

Photodiode capacitance changes significantly with bias voltage. With a 3.3V supply voltage, the reverse voltage on the PIN diode is only 2.5V. If a higher voltage supply is available, apply it to the diode to significantly reduce capacitance.

Take great care to reduce input capacitance. With the SO and µMAX versions of the MAX3664, the package capacitance is about 0.3pF, and the PC board between the MAX3664 input and the photodiode can add parasitic capacitance. Keep the input line short, and remove power and ground planes beneath it. Packaging the MAX3664 into a header with the photodiode provides the best possible performance. It reduces parasitic capacitance to a minimum, resulting in the lowest noise and the best bandwidth.

INREF1 and INREF2

Connect INREF1 and INREF2 as close to the AC ground of the photodetector diode as possible. The photodetector AC ground is usually the ground of the filter capacitor from the photodetector anode. The total loop (from INREF1/INREF2, through the bypass capacitor and the diode, and back to IN) should be no more than 2 cm. long.

Wire Bonding

For high current density and reliable operation, the MAX3664 uses gold metallization. Make connections to the die with gold wire only, and use ball bonding techniques (wedge bonding is not recommended). Die-pad size is 4 mils square, with a 6 mil pitch. Die thickness is 12 mils.

V_{CC} and Ground

Use good high-frequency design and layout techniques. The use of a multilayer circuit board with separate ground and V_{CC} planes is recommended. Take care to bypass V_{CC} and to connect the GND pin to the ground plane with the shortest possible traces.

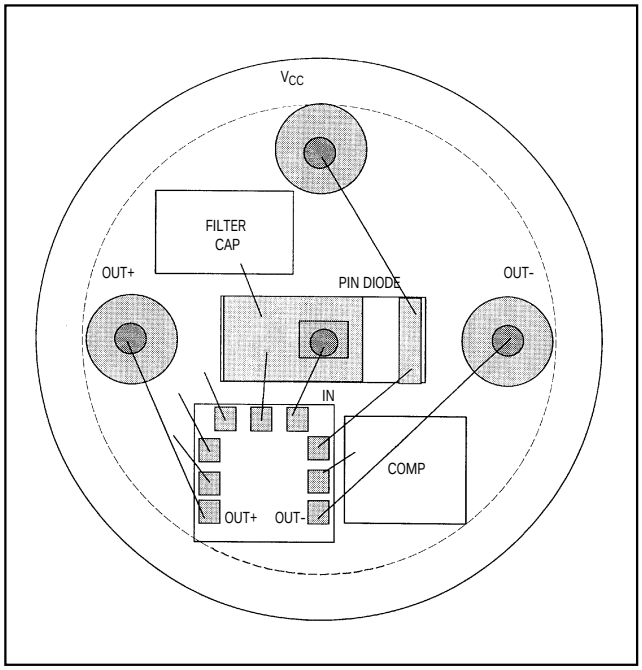
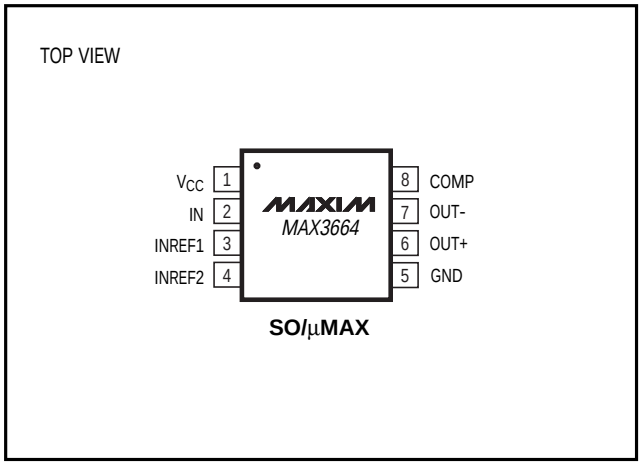


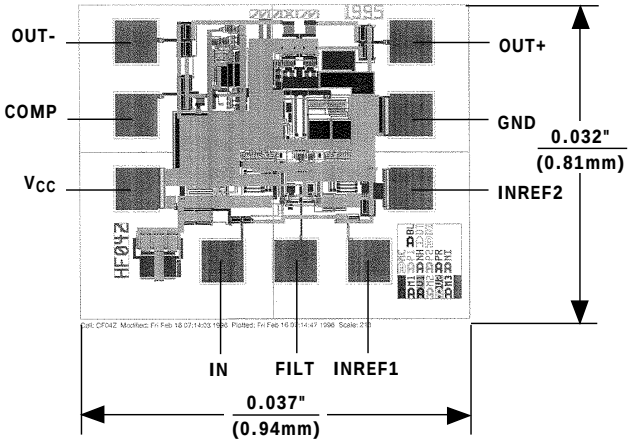
Figure 4. Suggested Layout for TO-46 Header

622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

Pin Configuration



Chip Topography

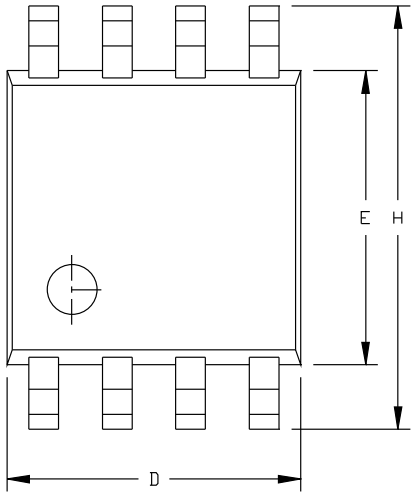


TRANSISTOR COUNT: 73

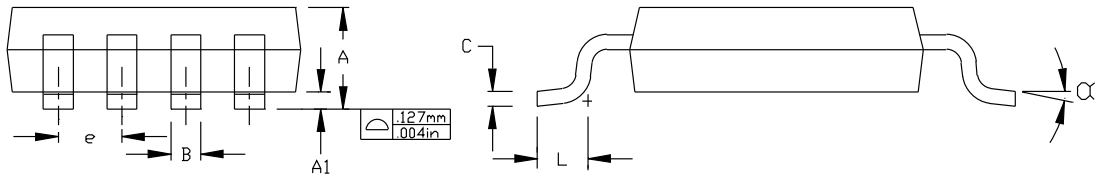
SUBSTRATE CONNECTED TO GND

Package Information

8LUMAXD.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256		0.65	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°



NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm(.006").
3. CONTROLLING DIMENSION: INCHES

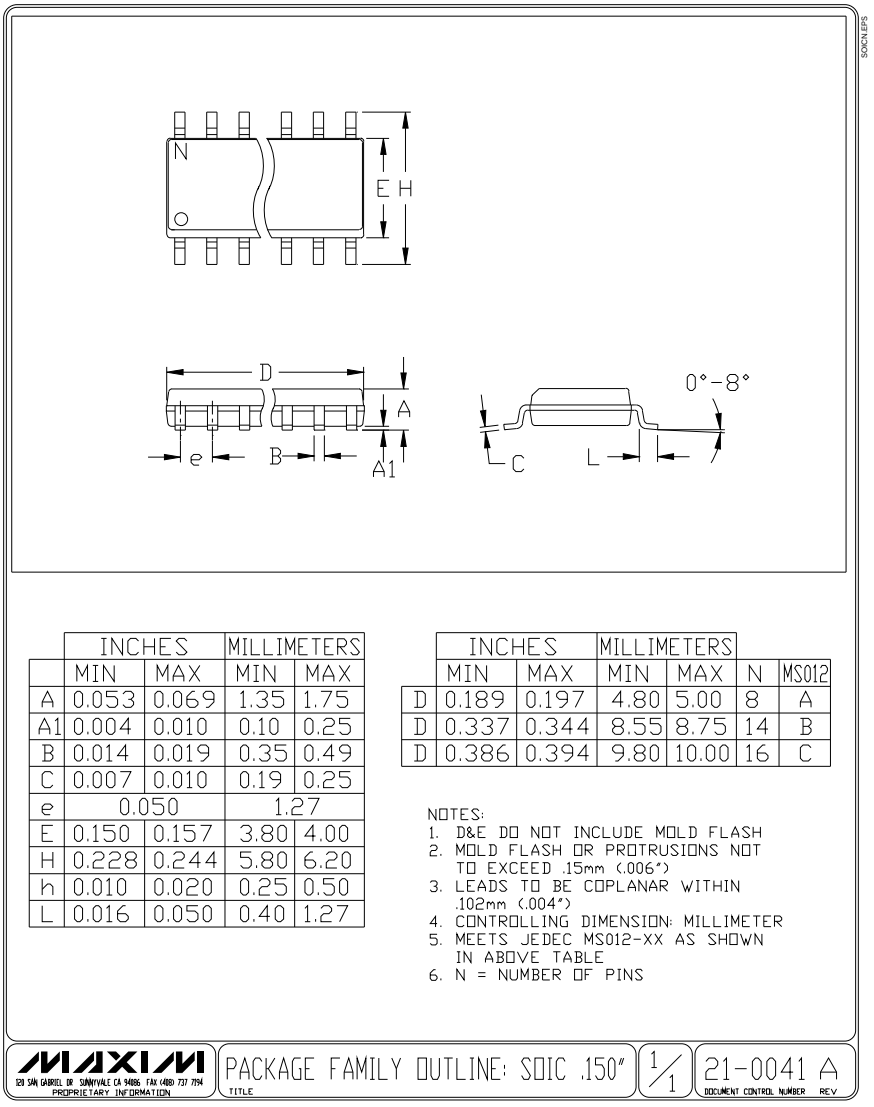
MAXIM
PROPRIETARY INFORMATION

TITLE:
8LD uMAX PACKAGE OUTLINE DWG.

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0036	D	1/1

622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

TITLE: PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | 21-0041 A (DOCUMENT CONTROL NUMBER REV)