

DATA SHEET

BFG410W

NPN 22 GHz wideband transistor

Product specification
Supersedes data of 1997 Oct 29

1998 Mar 11



NPN 22 GHz wideband transistor

BFG410W

FEATURES

- Very high power gain
- Low noise figure
- High transition frequency
- Emitter is thermal lead
- Low feedback capacitance.

APPLICATIONS

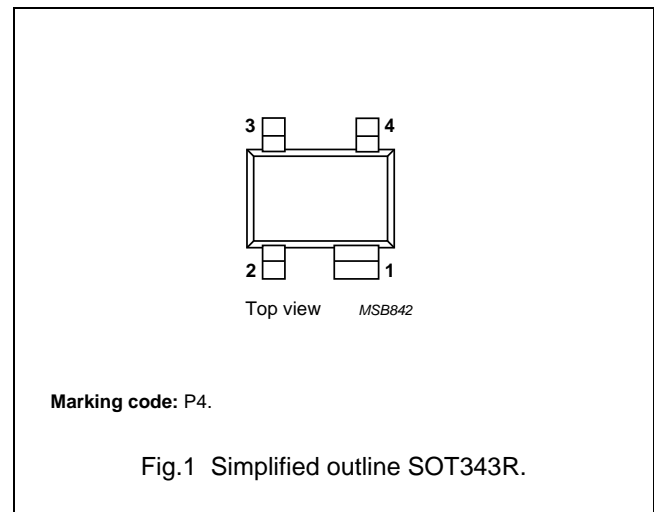
- RF front end
- Wideband applications, e.g. analog and digital cellular telephones, cordless telephones (PHS, DECT, etc.)
- Radar detectors
- Pagers
- Satellite television tuners (SATV)
- High frequency oscillators.

DESCRIPTION

NPN double polysilicon wideband transistor with buried layer for low voltage applications in a plastic, 4-pin dual-emitter SOT343R package.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	emitter
4	collector



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CB0}	collector-base voltage	open emitter	–	–	10	V
V_{CEO}	collector-emitter voltage	open base	–	–	4.5	V
I_C	collector current (DC)		–	10	12	mA
P_{tot}	total power dissipation	$T_s \leq 110\text{ }^\circ\text{C}$	–	–	54	mW
h_{FE}	DC current gain	$I_C = 10\text{ mA}; V_{CE} = 2\text{ V}; T_j = 25\text{ }^\circ\text{C}$	50	80	120	
C_{re}	feedback capacitance	$I_C = 0; V_{CB} = 2\text{ V}; f = 1\text{ MHz}$	–	45	–	fF
f_T	transition frequency	$I_C = 10\text{ mA}; V_{CE} = 2\text{ V}; f = 2\text{ GHz}; T_{amb} = 25\text{ }^\circ\text{C}$	–	22	–	GHz
G_{max}	maximum power gain	$I_C = 10\text{ mA}; V_{CE} = 2\text{ V}; f = 2\text{ GHz}; T_{amb} = 25\text{ }^\circ\text{C}$	–	21	–	dB
F	noise figure	$I_C = 1\text{ mA}; V_{CE} = 2\text{ V}; f = 2\text{ GHz}; \Gamma_S = \Gamma_{opt}$	–	1.2	–	dB

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

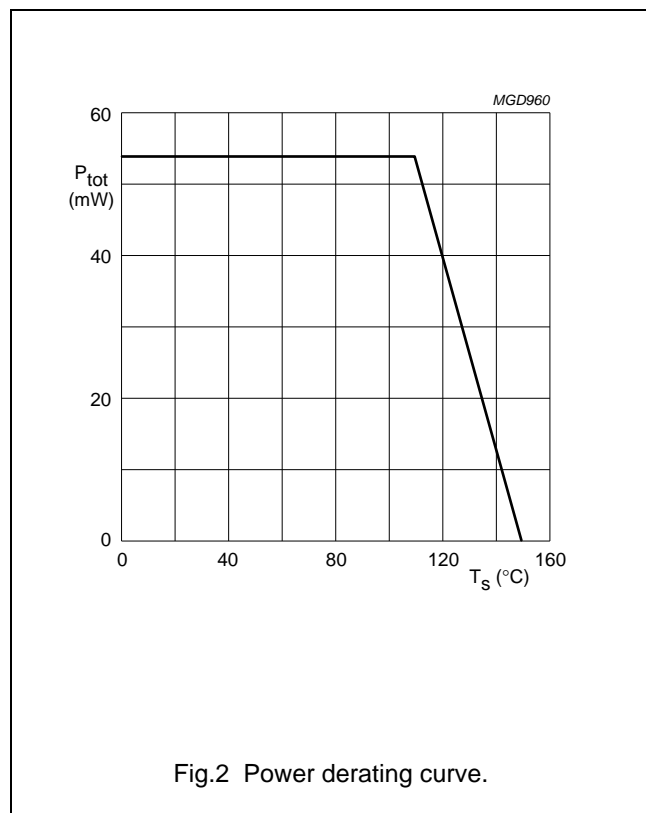
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	10	V
V _{CEO}	collector-emitter voltage	open base	–	4.5	V
V _{EBO}	emitter-base voltage	open collector	–	1	V
I _C	collector current (DC)		–	12	mA
P _{tot}	total power dissipation	T _s ≤ 110 °C; note 1; see Fig.2	–	54	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	operating junction temperature		–	150	°C

Note

1. T_s is the temperature at the soldering point of the emitter pins.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-s}	thermal resistance from junction to soldering point	750	K/W



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CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

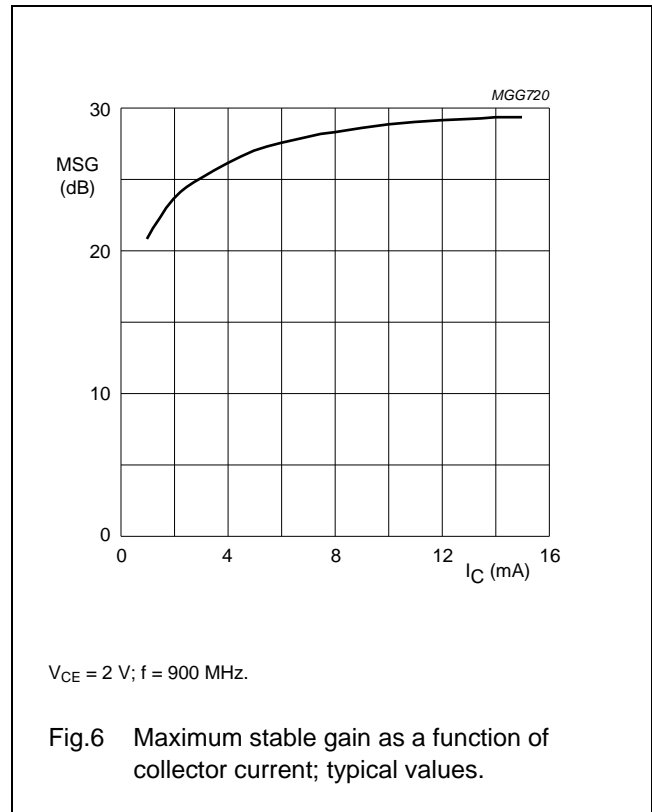
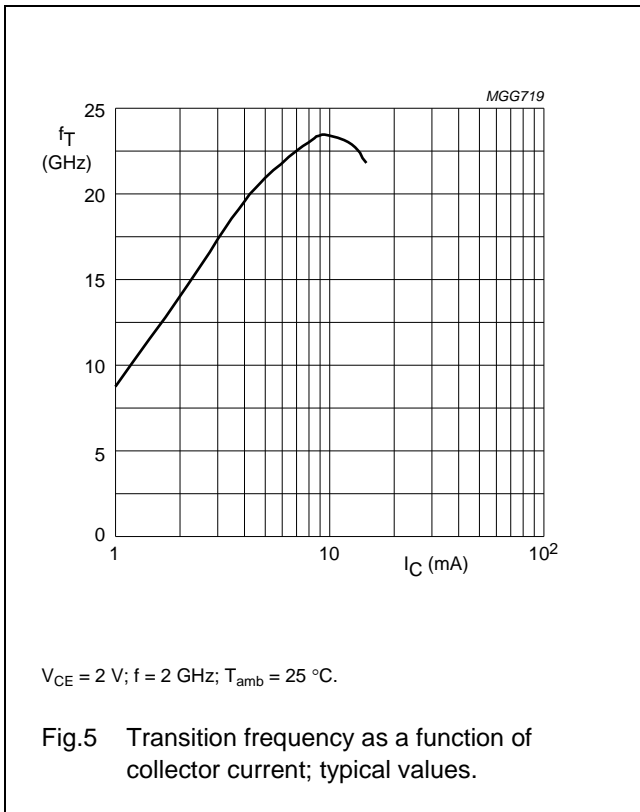
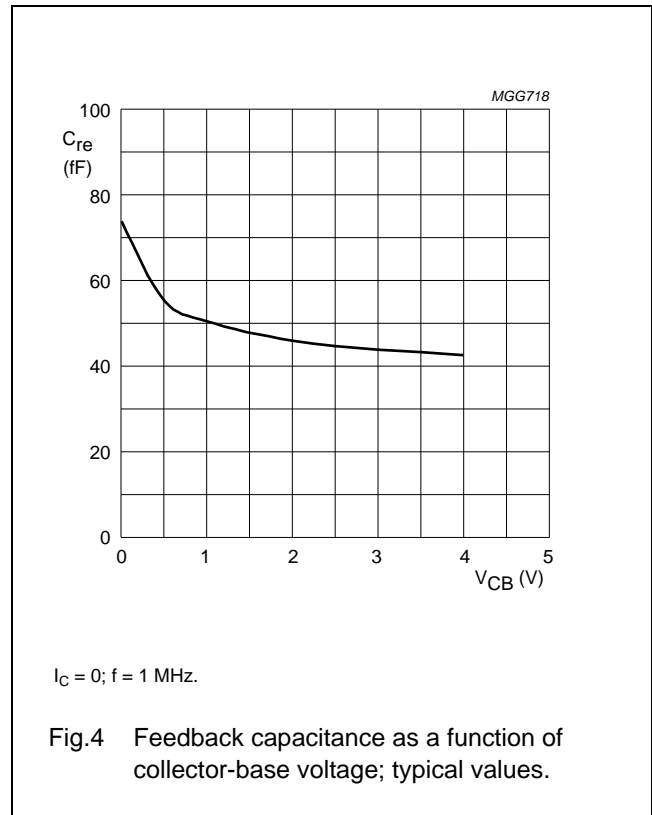
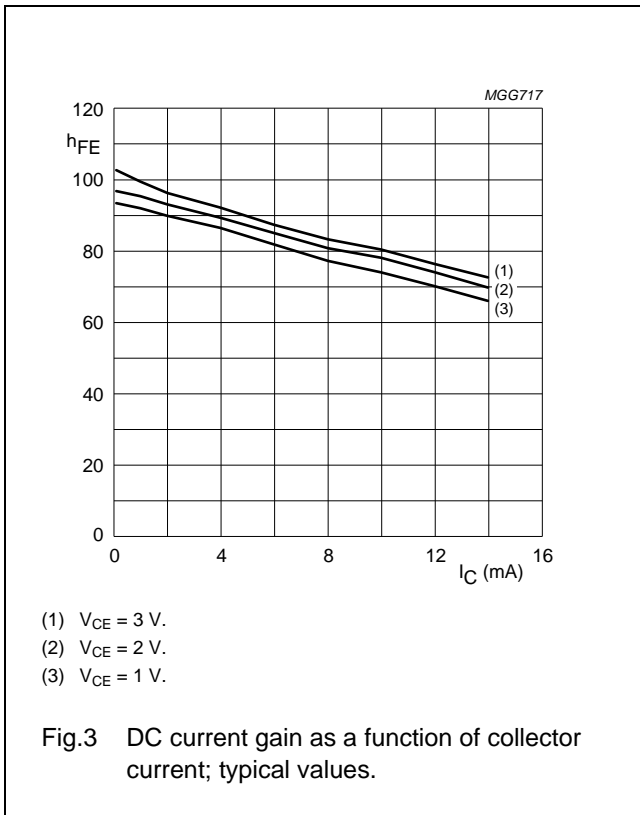
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 2.5\ \mu\text{A}; I_E = 0$	10	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 1\ \text{mA}; I_B = 0$	4.5	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	$I_E = 2.5\ \mu\text{A}; I_C = 0$	1	–	–	V
I_{CBO}	collector-base leakage current	$I_E = 0; V_{CB} = 4.5\ \text{V}$	–	–	15	nA
h_{FE}	DC current gain	$I_C = 10\ \text{mA}; V_{CE} = 2\ \text{V};$ see Fig.3	50	80	120	
C_c	collector capacitance	$I_E = i_e = 0; V_{CB} = 2\ \text{V}; f = 1\ \text{MHz}$	–	220	–	fF
C_e	emitter capacitance	$I_C = i_c = 0; V_{EB} = 0.5\ \text{V}; f = 1\ \text{MHz}$	–	400	–	fF
C_{re}	feedback capacitance	$I_C = 0; V_{CB} = 2\ \text{V}; f = 1\ \text{MHz};$ see Fig.4	–	45	–	fF
f_T	transition frequency	$I_C = 10\ \text{mA}; V_{CE} = 2\ \text{V}; f = 2\ \text{GHz};$ $T_{amb} = 25\text{ °C};$ see Fig.5	–	22	–	GHz
G_{max}	maximum power gain; note 1	$I_C = 10\ \text{mA}; V_{CE} = 2\ \text{V}; f = 2\ \text{GHz};$ $T_{amb} = 25\text{ °C};$ see Figs 7 and 8	–	21	–	dB
$ S_{21} ^2$	insertion power gain	$I_C = 10\ \text{mA}; V_{CE} = 2\ \text{V}; f = 2\ \text{GHz};$ $T_{amb} = 25\text{ °C};$ see Fig.8	–	18	–	dB
F	noise figure	$I_C = 1\ \text{mA}; V_{CE} = 2\ \text{V};$ $f = 900\ \text{MHz}; \Gamma_S = \Gamma_{opt};$ see Fig.13	–	0.9	–	dB
		$I_C = 1\ \text{mA}; V_{CE} = 2\ \text{V}; f = 2\ \text{GHz};$ $\Gamma_S = \Gamma_{opt};$ see Fig.13	–	1.2	–	dB
P_{L1}	output power at 1 dB gain compression	$I_C = 10\ \text{mA}; V_{CE} = 2\ \text{V}; f = 2\ \text{GHz};$ $Z_S = Z_{S\ opt}; Z_L = Z_{L\ opt};$ note 2	–	5	–	dBm
ITO	third order intercept point	$I_C = 10\ \text{mA}; V_{CE} = 2\ \text{V}; f = 2\ \text{GHz};$ $Z_S = Z_{S\ opt}; Z_L = Z_{L\ opt};$ note 2	–	15	–	dBm

Notes

- G_{max} is the maximum power gain, if $K > 1$. If $K < 1$ then $G_{max} = \text{MSG}$; see Figs 6, 7 and 8.
- Z_S is optimized for noise; Z_L is optimized for gain.

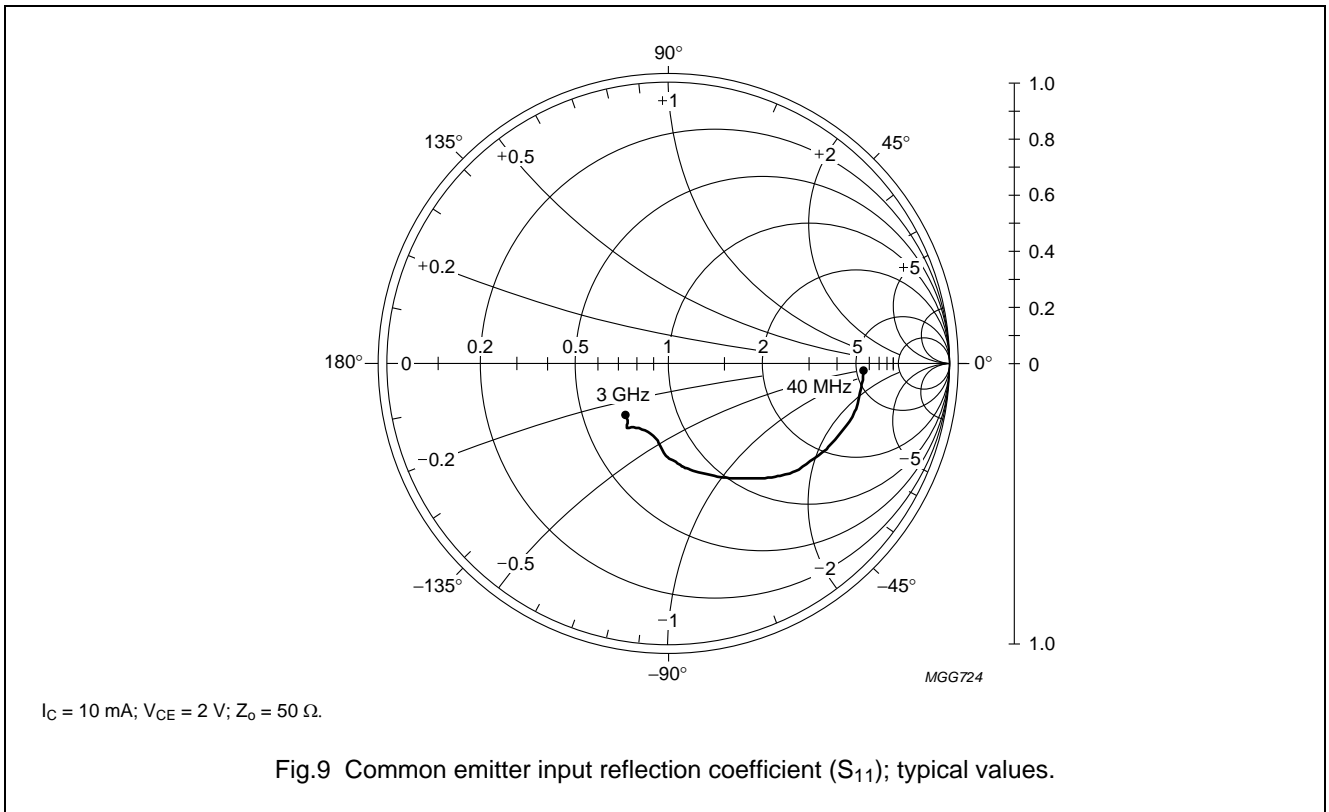
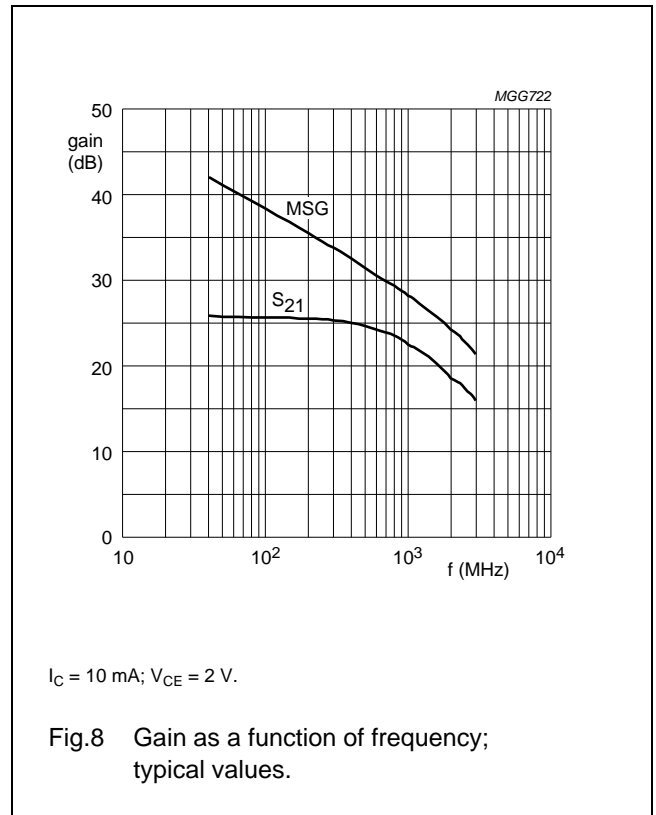
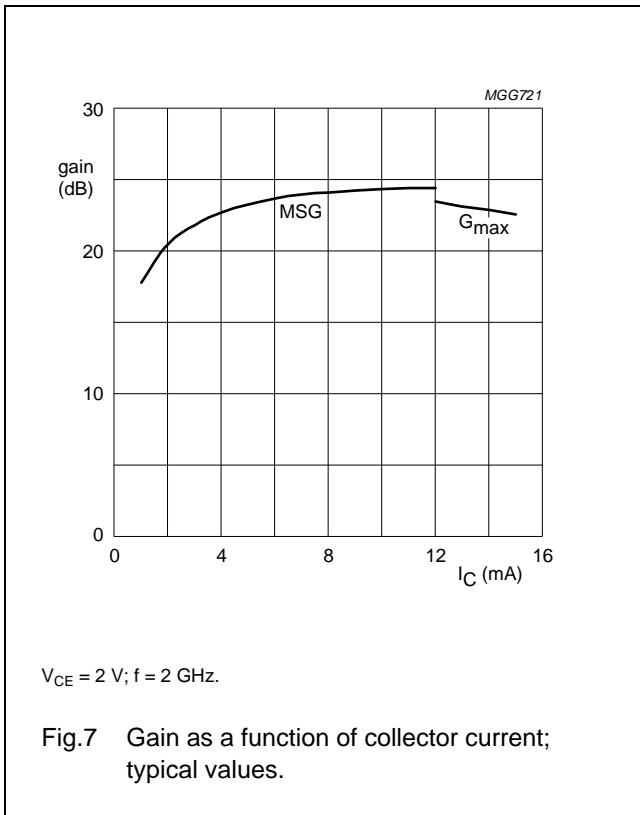
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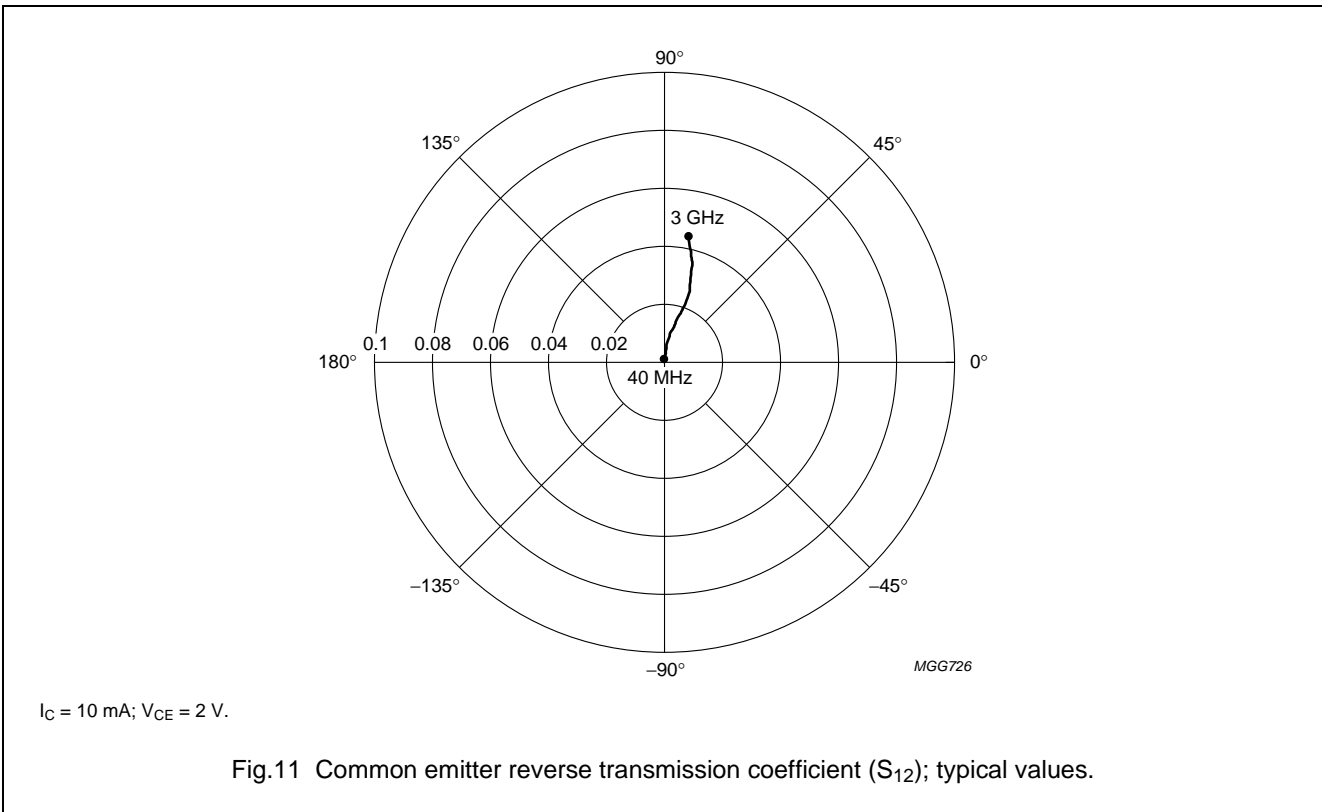
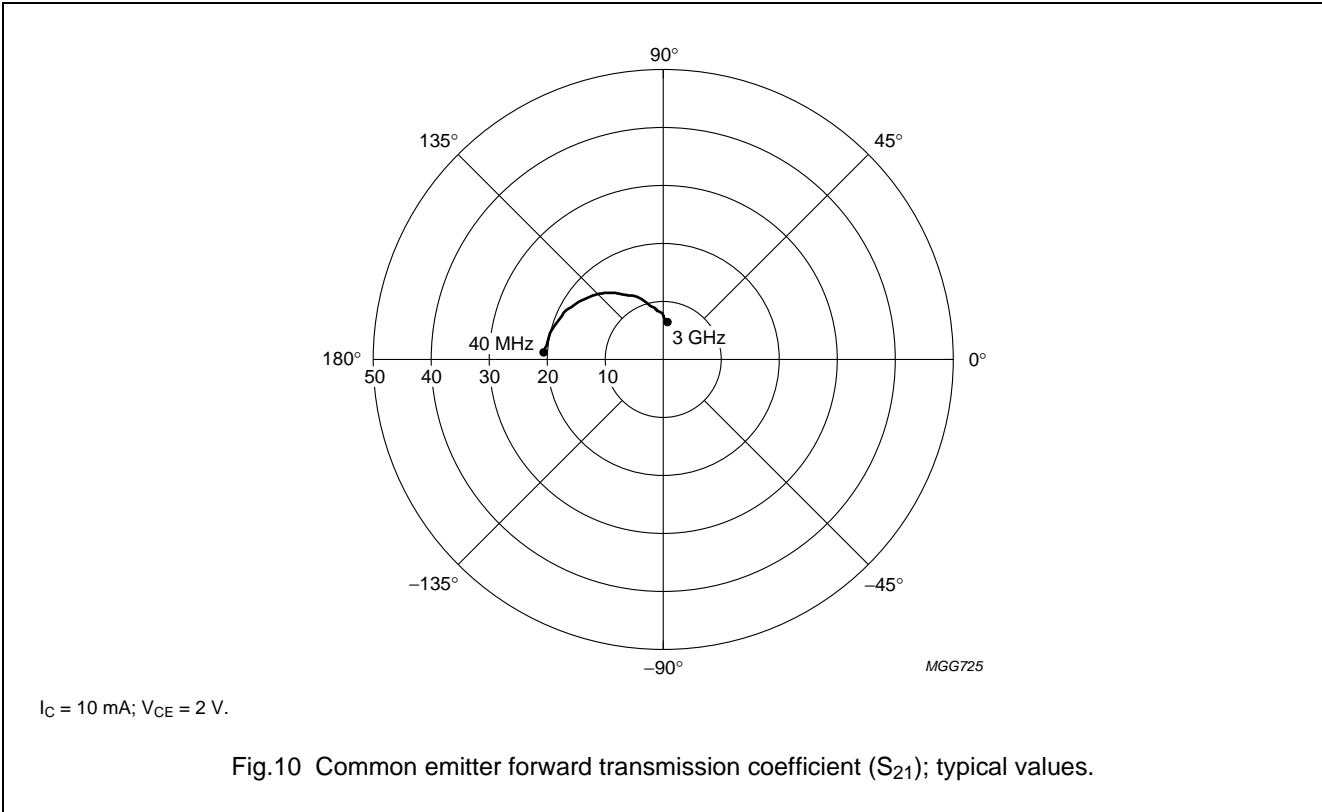
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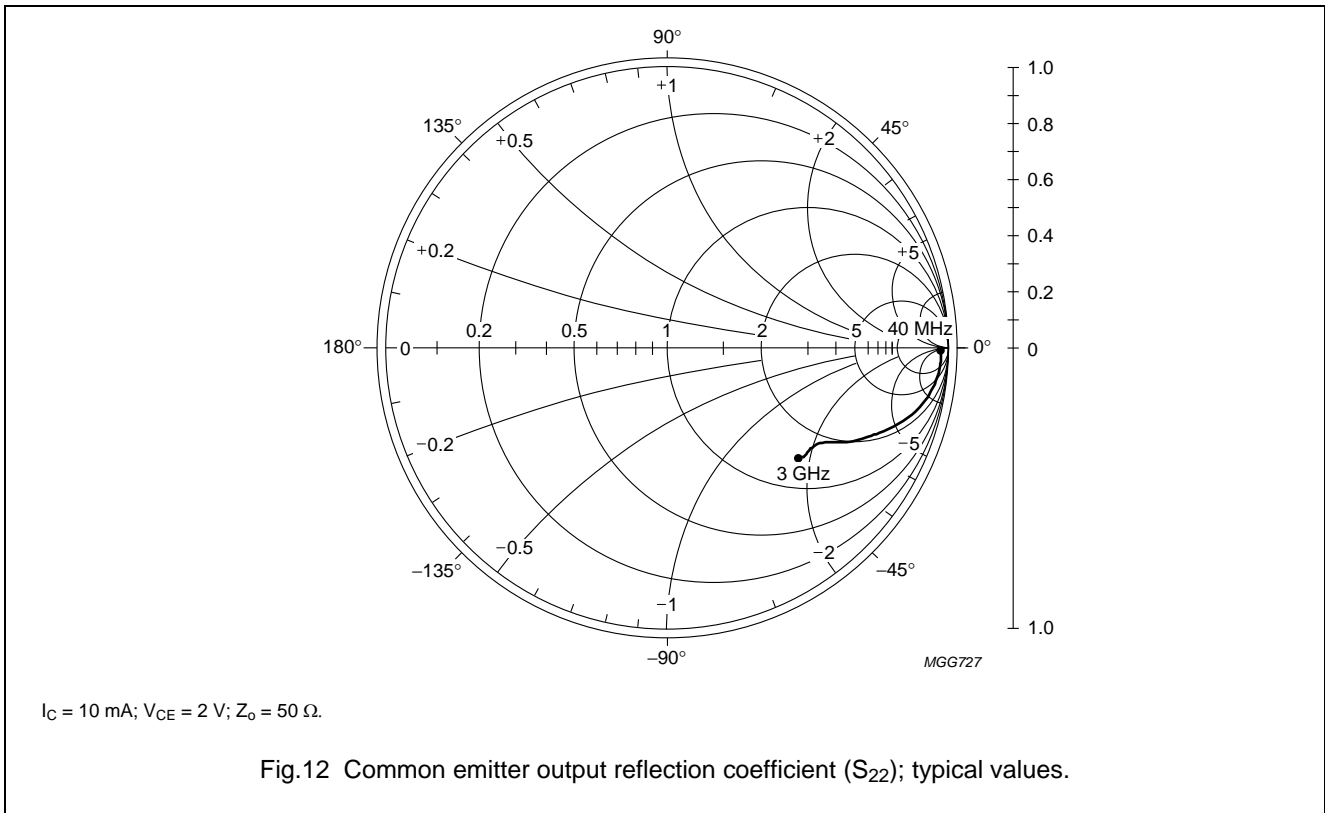
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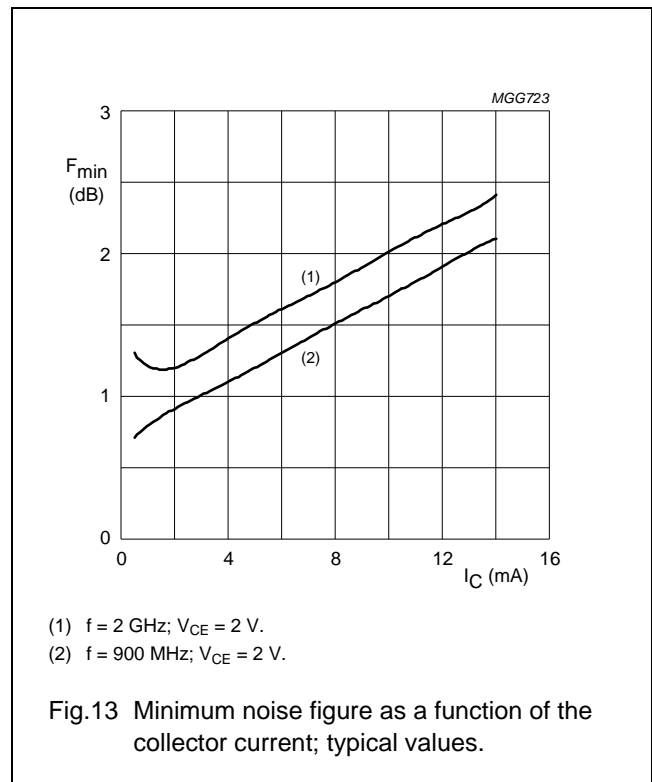
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Noise data

$V_{CE} = 2 \text{ V}$; typical values.

f (MHz)	I_C (mA)	F_{min} (dB)	Γ_{mag}	Γ_{angle}	r_n (Ω)
900	1	0.8	0.73	11.2	0.56
	2	0.9	0.58	10.1	0.43
	4	1.1	0.40	10.1	0.33
	6	1.3	0.28	11.0	0.30
	8	1.5	0.20	8.0	0.30
	10	1.7	0.14	10.5	0.27
	12	1.9	0.06	10.1	0.25
	14	2.1	0.05	14.2	0.26
2000	1	1.2	0.64	35.7	0.57
	2	1.2	0.50	35.8	0.44
	4	1.4	0.34	34.4	0.37
	6	1.6	0.25	33.7	0.34
	8	1.8	0.17	34.5	0.35
	10	2.0	0.12	35.8	0.34
	12	2.2	0.05	38.0	0.35
	14	2.4	0.03	44.8	0.34



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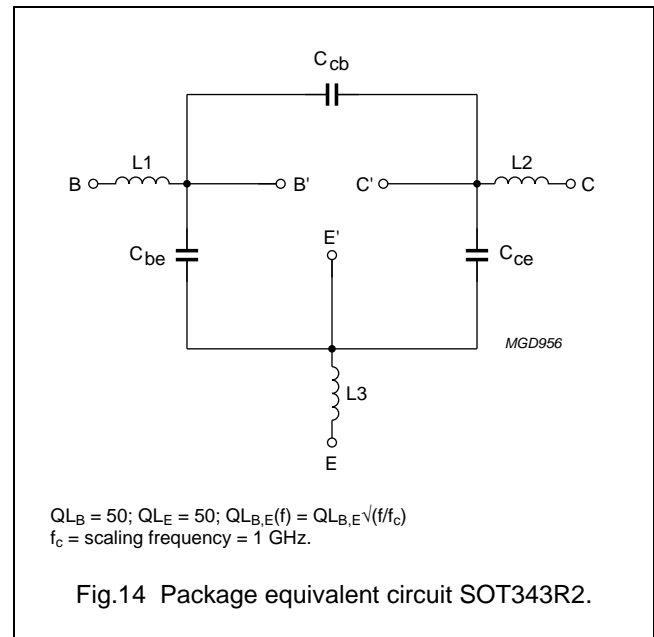
SPICE parameters for the BFG410W die

SEQUENCE No.	PARAMETER	VALUE	UNIT
1	IS	19.42	aA
2	BF	145.0	–
3	NF	0.993	–
4	VAF	31.12	V
5	IKF	125.0	mA
6	ISE	123.6	fA
7	NE	3.000	–
8	BR	11.37	–
9	NR	0.985	–
10	VAR	1.874	V
11	IKR	50.00	mA
12	ISC	199.6	aA
13	NC	1.546	–
14	RB	35.00	Ω
15	IRB	0.000	A
16	RBM	15.00	Ω
17	RE	432.0	mΩ
18	RC	4.324	Ω
19 (1)	XTB	1.500	–
20 (1)	EG	1.110	eV
21 (1)	XTI	3.000	–
22	CJE	128.0	fF
23	VJE	900.0	mV
24	MJE	0.346	–
25	TF	4.122	ps
26	XTF	68.20	–
27	VTF	2.004	V
28	ITF	0.627	A
29	PTF	0.000	deg
30	CJC	56.68	fF
31	VJC	556.9	mV
32	MJC	0.207	–
33	XCJC	0.500	–
34 (1)	TR	0.000	ns
35 (1)	CJS	274.8	fF
36 (1)	VJS	418.3	mV
37 (1)	MJS	0.239	–
38	FC	0.550	–

SEQUENCE No.	PARAMETER	VALUE	UNIT
39 (2)(3)	C _{bp}	145	fF
40 (2)	R _{sb1}	25	Ω
41 (3)	R _{sb2}	19	Ω

Notes

1. These parameters have not been extracted, the default values are shown.
2. Bonding pad capacity C_{bp} in series with substrate resistance R_{sb1} between B' and E'.
3. Bonding pad capacity C_{bp} in series with substrate resistance R_{sb2} between C' and E'.



List of components (see Fig.14)

DESIGNATION	VALUE	UNIT
C _{be}	80	fF
C _{cb}	2	fF
C _{ce}	80	fF
L1	1.1	nH
L2	1.1	nH
L3 (note 1)	0.25	nH

Note

1. External emitter inductance to be added separately due to the influence of the printed-circuit board.

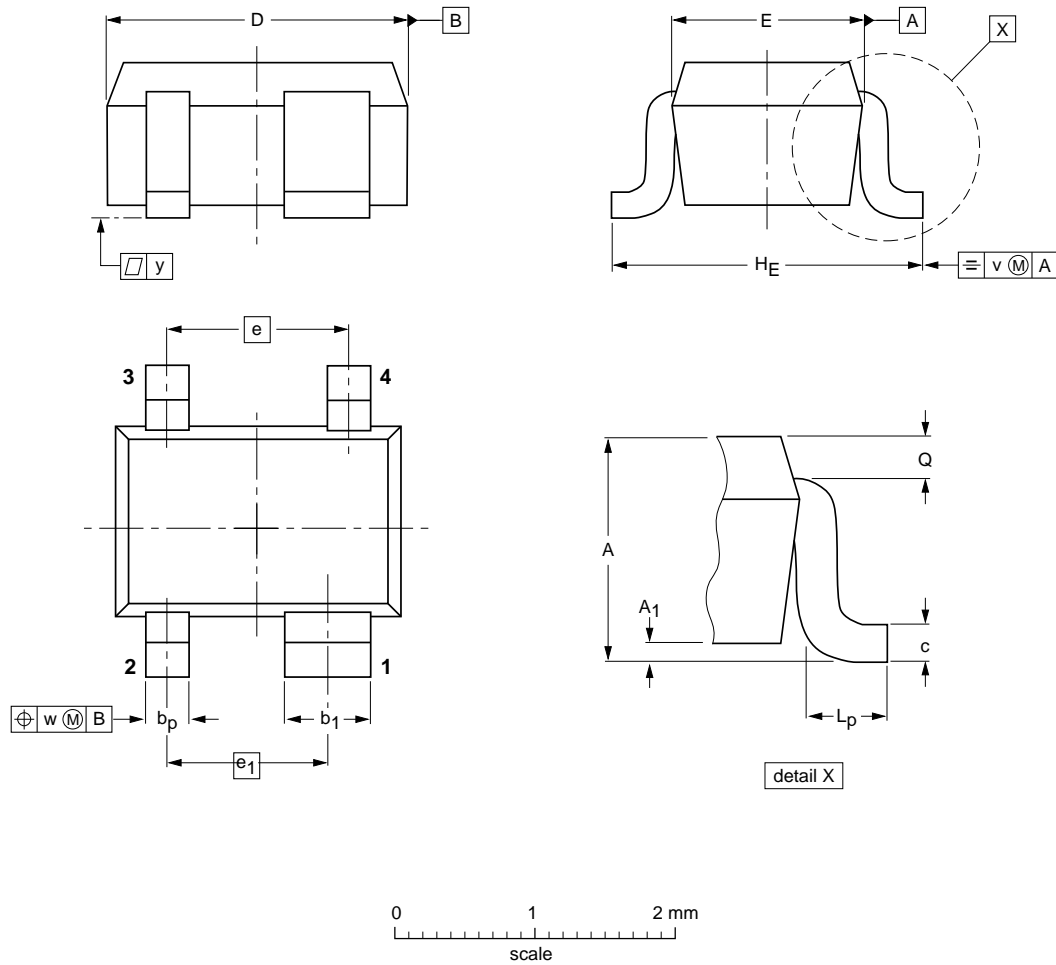
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PACKAGE OUTLINE

Plastic surface-mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21 06-03-16

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DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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