

General Description

The 932SQ428 is a main clock synthesizer for Romley-generation Intel based server platforms. The 932SQ428 is driven with a 25 MHz crystal for maximum performance. It generates CPU outputs of 100MHz.

Recommended Application

CK420BQ

Output Features

- 2 - HCSL Non-Spread SAS outputs
- 3 - HCSL SRC outputs - can be used as CPU@100M
- 1 - HCSL DOT96 output
- 1 - 3.3V 48M output
- 5 - 3.3V PCI outputs
- 1 - 3.3V 14.318M output

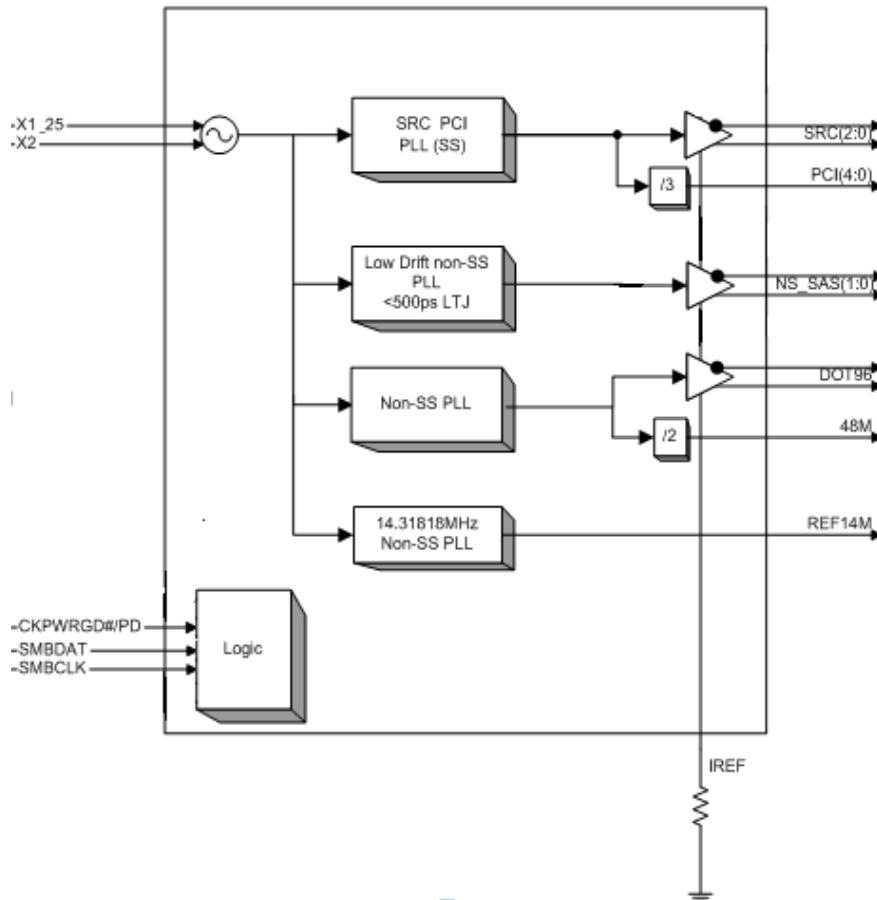
Features/Benefits

- 0.5% down spread capable on SRC/PCI outputs; Lower EMI
- 48-pin MLF package; Space Savings

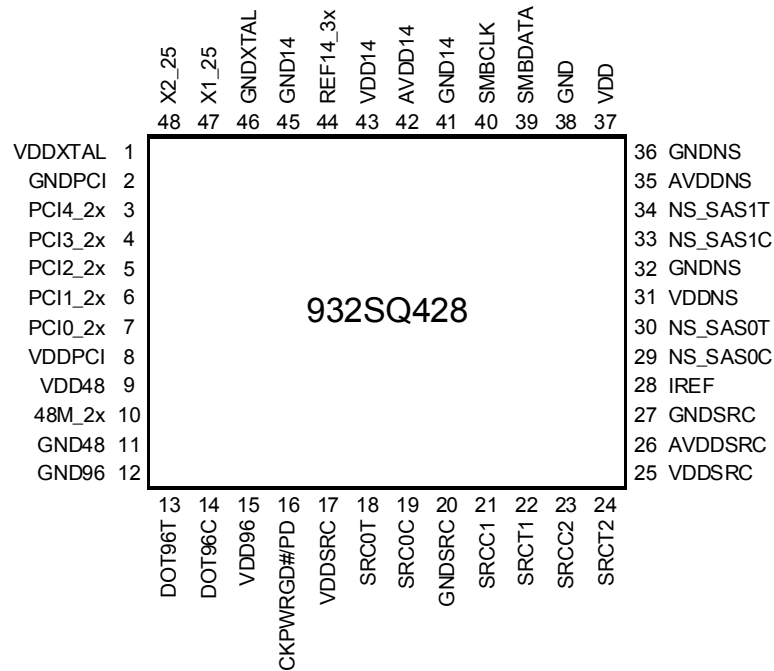
Key Specifications

- Cycle to cycle jitter: SRC/NS_SAS < 50ps
- Phase jitter: PCIe Gen2 <3ps rms
- Phase jitter: PCIe Gen3 <1ps rms
- Phase jitter: QPI 9.6GB/s <0.2ps rms
- Phase jitter: NS-SAS <0.4ps rms using raw phase data
- Phase jitter: NS-SAS <1.3ps rms using Clk Jit Tool 1.6.3

Block Diagram



Pin Configuration



48-Pin MLF (6x6mm 0.4mm pitch)

Pins with ^ prefix have internal 120K pullup
Pins with v prefix have internal 120K pulldown

932SQ428 Functionality

| SRC | PCI | REF | NS_SAS | DOT96 | USB | Unit |
|-----|-------|--------|--------|-------|-------|------|
| 100 | 33.33 | 14.318 | 100.00 | 96.00 | 48.00 | MHz |

Spread Spectrum Control

| SS_Enable (B1b0) | SRC & PCI |
|------------------|-----------|
| 0 | OFF |
| 1 | ON |

Power Group Table

| MLF | | Description |
|--------|-----|--|
| VDD | GND | |
| 42 | 41 | 14MHz PLL Analog |
| 43 | 45 | REF14M Output and Logic |
| 1 | 46 | 25MHz XTAL |
| 8 | 2 | PCI Outputs and Logic |
| 9 | 11 | 48MHz Output and Logic |
| 15 | 12 | 96MHz PLL Analog, Output and Logic |
| 17, 25 | 20 | SRC Outputs and Logic |
| 26 | 27 | SRC PLL Analog |
| 31 | 32 | Non-Spreading Differential Outputs & Logic |
| 35 | 36 | NS-SAS PLL Analog |
| 37 | 38 | Core Logic |

932SQ428 Power Down Functionality

| CKPWRGD#/PD | Differential Outputs | Single-ended Outputs | Single ended Outputs w/Latch |
|-------------|----------------------|----------------------|------------------------------|
| 1 | HI-Z ¹ | Low | Low ² |
| 0 | Running | | |

1. Hi-Z on the differential outputs will result in both True and Complement being low due to the termination network
2. These outputs are Hi-Z after VDD is applied and before the first assertion of CKPWRGD#.

Pin Descriptions

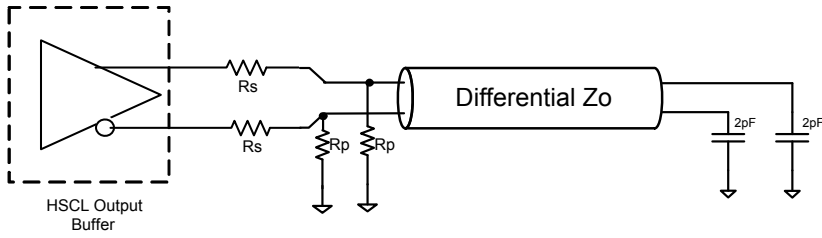
| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|-------------|------|---|
| 1 | VDDXTAL | PWR | 3.3V power for the crystal oscillator. |
| 2 | GNDPCI | PWR | Ground pin for PCI outputs and logic. |
| 3 | PCI4_2x | OUT | 3.3V PCI clock output |
| 4 | PCI3_2x | OUT | 3.3V PCI clock output |
| 5 | PCI2_2x | OUT | 3.3V PCI clock output |
| 6 | PCI1_2x | OUT | 3.3V PCI clock output |
| 7 | PCI0_2x | OUT | 3.3V PCI clock output |
| 8 | VDDPCI | PWR | 3.3V power for the PCI outputs and logic |
| 9 | VDD48 | PWR | 3.3V power for the 48MHz output and logic |
| 10 | 48M_2x | OUT | 3.3V 48MHz output |
| 11 | GND48 | PWR | Ground pin for 48MHz output and logic. |
| 12 | GND96 | PWR | Ground pin for DOT96 output and logic. |
| 13 | DOT96T | OUT | True clock of differential 96MHz output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 14 | DOT96C | OUT | Complementary clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 15 | VDD96 | PWR | 3.3V power for the 48/96MHz PLL and the 96MHz output and logic |
| 16 | CKPWRGD#/PD | IN | CKPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped. |
| 17 | VDDSRC | PWR | 3.3V power for the SRC outputs and logic |
| 18 | SRC0T | OUT | True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 19 | SRC0C | OUT | Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 20 | GNDSRC | PWR | Ground pin for SRC outputs and logic. |
| 21 | SRCC1 | OUT | Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 22 | SRCT1 | OUT | True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 23 | SRCC2 | OUT | Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 24 | SRCT2 | OUT | True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 25 | VDDSRC | PWR | 3.3V power for the SRC outputs and logic |
| 26 | AVDDSRC | PWR | 3.3V power for the SRC PLL analog circuits |
| 27 | GNDSRC | PWR | Ground pin for SRC outputs and logic. |
| 28 | IREF | OUT | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 29 | NS_SAS0C | OUT | Complementary clock of differential non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 30 | NS_SAS0T | OUT | True clock of differential non-spreading SAS output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 31 | VDDNS | PWR | 3.3V power for the Non-Spreading differential outputs outputs and logic |
| 32 | GNDNS | PWR | Ground pin for non-spreading differential outputs and logic. |
| 33 | NS_SAS1C | OUT | Complementary clock of differential non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |
| 34 | NS_SAS1T | OUT | True clock of differential non-spreading SAS output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. |

Pin Descriptions (cont.)

| | | | |
|----|----------|-----|--|
| 35 | AVDDNS | PWR | 3.3V power for the non-spreading SAS PLL analog circuits. |
| 36 | GNDNS | PWR | Ground pin for non-spreading differential outputs and logic. |
| 37 | VDD | PWR | 3.3V power for core logic |
| 38 | GND | PWR | Ground pin for core logic. |
| 39 | SMBDATA | I/O | Data pin of SMBUS circuitry, 5V tolerant |
| 40 | SMBCLK | IN | Clock pin of SMBUS circuitry, 5V tolerant |
| 41 | GND14 | PWR | Ground pin for 14MHz output and logic. |
| 42 | AVDD14 | PWR | Analog power pin for 14MHz PLL |
| 43 | VDD14 | PWR | Power pin for 14MHz output and logic, nominal 3.3V |
| 44 | REF14_3x | OUT | 14.318 MHz reference clock. 3X drive strength as default |
| 45 | GND14 | PWR | Ground pin for 14MHz output and logic. |
| 46 | GNDXTAL | PWR | Ground pin for Crystal Oscillator. |
| 47 | X1_25 | IN | Crystal input, Nominally 25.00MHz. |
| 48 | X2_25 | OUT | Crystal output, Nominally 25.00MHz. |

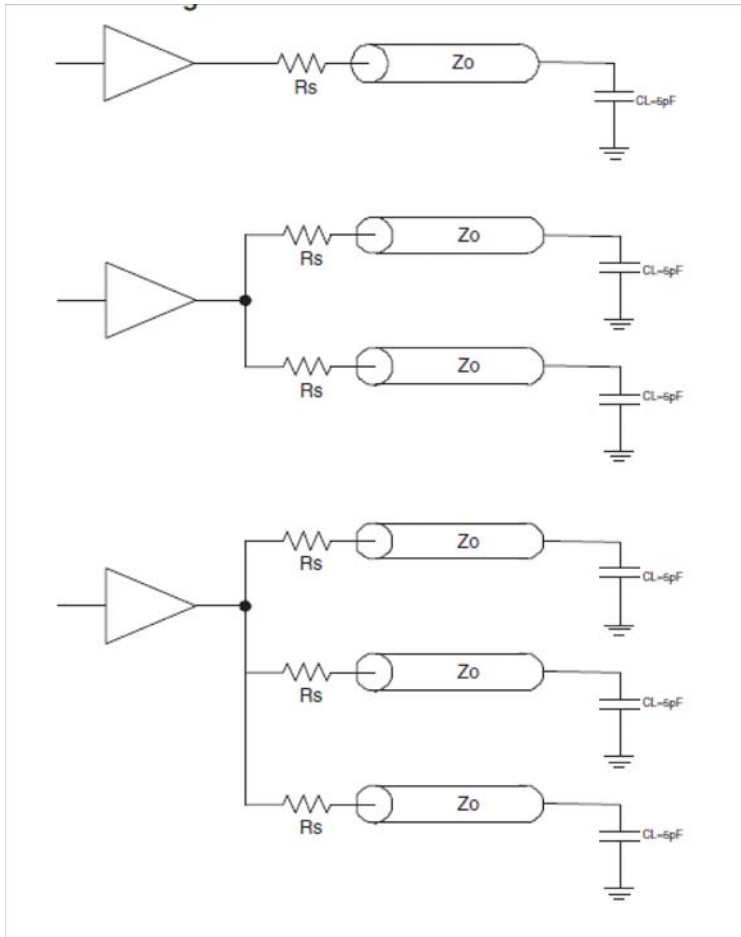
Test Loads and Recommended Terminations

932SQ428 Differential Test Loads



Differential Output Termination Table

| DIF Zo (Ω) | Iref (Ω) | Rs (Ω) | Rp (Ω) |
|---------------------|-------------------|-----------------|-----------------|
| 100 | 475 | 33 | 50 |
| 85 | 412 | 27 | 42.2 or 43.2 |



Single-ended Output Termination Table

| Output | Loads | Rs Value (for each load) | |
|---------|-------|-----------------------------|------------------|
| | | Zo = 50 Ω | Zo = 60 Ω |
| PCI/USB | 1 | 36 | 43 |
| PCI/USB | 2 | 22 | 33 |
| REF | 1 | 39 | 47 |
| REF | 2 | 27 | 36 |
| REF | 3 | 10 | 20 |

Electrical Characteristics - Absolute Maximum Ratings

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|--------------------|----------------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Core Supply Voltage | VDDA | | | | 4.6 | V | 1,2 |
| 3.3V Logic Supply Voltage | VDD | | | | 4.6 | V | 1,2 |
| Input Low Voltage | V _{IL} | | GND-0.5 | | | V | 1 |
| Input High Voltage | V _{IH} | Except for SMBus interface | | | V _{DD} +0.5V | V | 1 |
| Input High Voltage | V _{IHSMB} | SMBus clock and data pins | | | 5.5V | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics - Current Consumption

T_A = T_{COM}; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|-----------------------|---|-----|-----|-----|-------|-------|
| Operating Supply Current | I _{DD3.30P} | All outputs active @100MHz, C _L = Full load; | | 250 | 300 | mA | 1 |
| Powerdown Current | I _{DD3.3PDZ} | All differential pairs tri-stated | | 12 | 20 | mA | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

DC Electrical Characteristics - Differential Current Mode Outputs

T_A = T_{COM}; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|------------|--|------|------|------|-------|---------|
| Slew rate | Trf | Scope averaging on | 1 | 2.4 | 4 | V/ns | 1, 2, 3 |
| Slew rate matching | ΔTrf | Slew rate matching, Scope averaging on | | 9 | 20 | % | 1, 2, 4 |
| Rise/Fall Time Variation | ΔTrf | Rise/fall variation, Scope averaging off | | 18 | 125 | ps | 1, 7, 8 |
| Voltage High | VHigh | Statistical measurement on single-ended signal using | 660 | 772 | 850 | mV | 1 |
| Voltage Low | VLow | | -150 | 9 | 150 | | 1 |
| Max Voltage | Vmax | Measurement on single ended signal using absolute value. | | 810 | 1150 | mV | 1, 7 |
| Min Voltage | Vmin | | -300 | -17 | | | 1, 7 |
| Vswing | Vswing | Scope averaging off | 300 | 1446 | | mV | 1, 2 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 250 | 351 | 550 | mV | 1, 5 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off | | 24 | 140 | mV | 1, 6 |

¹Guaranteed by design and characterization, not 100% tested in production. I_{REF} = VDD/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω (100Ω differential impedance).

² Measured from differential waveform

³ Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than V_cross absolute.

⁷ Includes overshoot and undershoot.

Electrical Characteristics - Input/Supply/Common Parameters

TA = T_{COM}; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|----------------------------------|---------------------|---|-----------------------|---------|-----------------------|-------|-------|
| Ambient Operating Temperature | T _{COM} | Commercial range | 0 | | 70 | °C | 1 |
| Input High Voltage | V _{IH} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | 2 | | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{IL} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | GND - 0.3 | | 0.8 | V | 1 |
| Input Current | I _{IN} | Single-ended inputs, V _{IN} = GND, V _{IN} = VDD | -5 | | 5 | uA | 1 |
| | I _{INP} | Single-ended inputs. V _{IN} = 0 V; Inputs with internal pull up resistors V _{IN} = VDD; Inputs with internal pull-down resistors | -200 | | 200 | uA | 1 |
| Low Threshold Input-High Voltage | V _{IH_FS} | 3.3 V +/-5% | 0.7 | | V _{DD} + 0.3 | V | 1 |
| Low Threshold Input-Low Voltage | V _{IL_FS} | 3.3 V +/-5% | V _{SS} - 0.3 | | 0.35 | V | 1 |
| Input Frequency | F _i | | | 25.00 | | MHz | 2 |
| Pin Inductance | L _{p.in} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs | | | 5 | pF | 1 |
| | C _{OUT} | Output pin capacitance | | | 5 | pF | 1 |
| | C _{INX} | X1 & X2 pins | | | 5 | pF | 1 |
| Clk Stabilization | T _{STAB} | From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | | 1.8 | ms | 1,2 |
| SS Modulation Frequency | f _{MODIN} | Allowable Frequency (Triangular Modulation) | 30 | 31.500 | 33 | kHz | 1 |
| Tdrive_PD# | t _{DRVPD} | Differential output enable after PD# de-assertion | | 200.000 | 300 | us | 1,3 |
| Tfall | t _F | Fall time of control inputs | | | 5 | ns | 1,2 |
| Trise | t _R | Rise time of control inputs | | | 5 | ns | 1,2 |
| SMBus Input Low Voltage | V _{ILSMB} | | | | 0.8 | V | 1 |
| SMBus Input High Voltage | V _{IHSMB} | | 2.1 | | V _{DDSMB} | V | 1 |
| SMBus Output Low Voltage | V _{OLSMB} | @ I _{PULLUP} | | | 0.4 | V | 1 |
| SMBus Sink Current | I _{PULLUP} | @ V _{OL} | 4 | | | mA | 1 |
| Nominal Bus Voltage | V _{DDSMB} | 3V to 5V +/- 10% | 2.7 | | 5.5 | V | 1 |
| SCLK/SDATA Rise Time | t _{RSMB} | (Max V _{IL} - 0.15) to (Min V _{IH} + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t _{FSMB} | (Min V _{IH} + 0.15) to (Max V _{IL} - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | f _{MAXSMB} | Maximum SMBus operating frequency | | | 100 | kHz | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

AC Electrical Characteristics - Differential Current Mode Outputs

$T_A = T_{COM}$; Supply Voltage $V_{DD} = 3.3\text{ V} \pm 5\%$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|---------------|--------------------------------------|-----|------|-----|-------|-------|
| Duty Cycle | t_{DC} | Measured differentially, PLL Mode | 45 | 50.1 | 55 | % | 1 |
| Skew, Output to Output | t_{sk3SRC} | Across all SRC outputs, $V_T = 50\%$ | | 13.5 | 50 | ps | 1 |
| Jitter, Cycle to cycle | $t_{jyc-cyc}$ | SRC, NS_SAS outputs | | 35 | 50 | ps | 1,3 |
| | | DOT96 output | | 75 | 250 | ps | 1,3 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² $I_{REF} = V_{DD}/(3 \times R_R)$. For $R_R = 475\Omega$ (1%), $I_{REF} = 2.32\text{mA}$. $I_{OH} = 6 \times I_{REF}$ and $V_{OH} = 0.7\text{V}$ @ $Z_O = 50\Omega$.

³ Measured from differential waveform

Electrical Characteristics - Phase Jitter Parameters

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD}/V_{DDA} = 3.3\text{ V} \pm 5\%$,

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|-----------------|-------------------|---|------|------|----------|----------|---------|
| Phase Jitter | $t_{jphPCleG1}$ | PCIe Gen 1 | | 28 | 86 | ps (p-p) | 1,2,3,6 |
| | $t_{jphPCleG2}$ | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.9 | 3 | ps (rms) | 1,2,6 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 1.7 | 3.1 | ps (rms) | 1,2,6 |
| | $t_{jphPCleG3}$ | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | | 0.4 | 1 | ps (rms) | 1,2,4,6 |
| | t_{jphQPI_SMI} | QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.15 | 0.5 | ps (rms) | 1,5,6 |
| | | QPI & SMI (100MHz, 8.0Gb/s, 12UI) | | 0.13 | 0.3 | ps (rms) | 1,5,6 |
| | | QPI & SMI (100MHz, 9.6Gb/s, 12UI) | | 0.11 | 0.2 | ps (rms) | 1,5,6 |
| | $t_{jphSAS12G}$ | SAS12G (Filtered REFCLK Jitter 20KHz to 20MHz.) | | 0.34 | 0.4 | ps (rms) | 1,7,8 |
| $t_{jphSAS12G}$ | SAS 12G | | 0.70 | 1.3 | ps (rms) | 1,5,7 | |

¹ Guaranteed by design and characterization, not 100% tested in production.

² See <http://www.pcisig.com> for complete specs

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ Subject to final radification by PCI SIG.

⁵ Calculated from Intel-supplied Clock Jitter Tool v 1.6.6

⁶ Applies to SRC outputs

⁷ Applies to NS_SAS, NS_SRC outputs, Spread Off

⁸ Intel calculation from raw phase noise data

Electrical Characteristics - PCI

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD}/V_{DDA} = 3.3\text{ V} \pm 5\%$,

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|---------------|---------------------------------|-----|------|------|----------|-------|
| Output Impedance | R_{DSP} | $V_O = V_{DD}^*(0.5)$ | 12 | | 55 | Ω | 1 |
| Output High Voltage | V_{OH} | $I_{OH} = -1\text{ mA}$ | 2.4 | | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{OL} = 1\text{ mA}$ | | | 0.55 | V | 1 |
| Output High Current | I_{OH} | MIN @ $V_{OH} = 1.0\text{ V}$ | -33 | | | mA | 1 |
| | | MAX @ $V_{OH} = 3.135\text{ V}$ | | | -33 | mA | 1 |
| Output Low Current | I_{OL} | MIN @ $V_{OL} = 1.95\text{ V}$ | 30 | | | mA | 1 |
| | | MAX @ $V_{OL} = 0.4\text{ V}$ | | | 38 | mA | 1 |
| Clock High Time | T_{HIGH} | 1.5V | 12 | | | ns | 1 |
| Clock Low Time | T_{LOW} | 1.5V | 12 | | | ns | 1 |
| Edge Rate | $t_{slew/f}$ | Rising/Falling edge rate | 1 | 1.8 | 4 | V/ns | 1,2 |
| Duty Cycle | d_{t1} | $V_T = 1.5\text{ V}$ | 45 | 50.5 | 55 | % | 1 |
| Group Skew | t_{skew} | $V_T = 1.5\text{ V}$ | | 294 | 500 | ps | 1 |
| Jitter, Cycle to cycle | $t_{jcy-cyc}$ | $V_T = 1.5\text{ V}$ | | 108 | 500 | ps | 1 |

See "Single-ended Test Loads Page" for termination circuits

¹Guaranteed by design and characterization, not 100% tested in production.

²Measured between 0.8V and 2.0V

Electrical Characteristics - 48MHz

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD}/V_{DDA} = 3.3\text{ V} \pm 5\%$,

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|-------------------|---------------------------------|-------|-----|--------|----------|-------|
| Output Impedance | R_{DSP} | $V_O = V_{DD}^*(0.5)$ | 20 | | 60 | Ω | 1 |
| Output High Voltage | V_{OH} | $I_{OH} = -1\text{ mA}$ | 2.4 | | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{OL} = 1\text{ mA}$ | | | 0.55 | V | 1 |
| Output High Current | I_{OH} | MIN @ $V_{OH} = 1.0\text{ V}$ | -29 | | | mA | 1 |
| | | MAX @ $V_{OH} = 3.135\text{ V}$ | | | -33 | mA | 1 |
| Output Low Current | I_{OL} | MIN @ $V_{OL} = 1.95\text{ V}$ | 29 | | | mA | 1 |
| | | MAX @ $V_{OL} = 0.4\text{ V}$ | | | 27 | mA | 1 |
| Clock High Time | T_{HIGH} | 1.5V | 8.094 | | 10.036 | ns | 1 |
| Clock Low Time | T_{LOW} | 1.5V | 7.694 | | 9.836 | ns | 1 |
| Edge Rate | t_{slew/f_USB} | Rising/Falling edge rate | 1 | 1.5 | 2 | V/ns | 1,2 |
| Duty Cycle | d_{t1} | $V_T = 1.5\text{ V}$ | 45 | 51 | 55 | % | 1 |
| Jitter, Cycle to cycle | $t_{jcy-cyc}$ | $V_T = 1.5\text{ V}$ | | 109 | 350 | ps | 1 |

See "Single-ended Test Loads Page" for termination circuits

¹Guaranteed by design and characterization, not 100% tested in production.

²Measured between 0.8V and 2.0V

Electrical Characteristics - REF

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD}/V_{DDA} = 3.3\text{ V} \pm 5\%$,

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|------------------------|-----------------------|---------------------------------|------|------|------|----------|-------|
| Output Impedance | R_{DSP} | $V_O = V_{DD}*(0.5)$ | 12 | | 55 | Ω | 1 |
| Output High Voltage | V_{OH} | $I_{OH} = -1\text{ mA}$ | 2.4 | | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{OL} = 1\text{ mA}$ | | | 0.55 | V | 1 |
| Output High Current | I_{OH} | MIN @ $V_{OH} = 1.0\text{ V}$ | -33 | | | mA | 1 |
| | | MAX @ $V_{OH} = 3.135\text{ V}$ | | | -33 | mA | 1 |
| Output Low Current | I_{OL} | MIN @ $V_{OL} = 1.95\text{ V}$ | 30 | | | mA | 1 |
| | | MAX @ $V_{OL} = 0.4\text{ V}$ | | | 38 | mA | 1 |
| Clock High Time | T_{HIGH} | 1.5V | 27.5 | | | ns | 1 |
| Clock Low Time | T_{LOW} | 1.5V | 27.5 | | | ns | 1 |
| Edge Rate | $t_{sle\ wr/f}$ | Rising/Falling edge rate | 1 | 1.9 | 4 | V/ns | 1,2 |
| Duty Cycle | d_{t1} | $V_T = 1.5\text{ V}$ | 45 | 50.5 | 55 | % | 1 |
| Jitter, Cycle to cycle | $t_{j\text{cyc-cyc}}$ | $V_T = 1.5\text{ V}$ | | 75 | 1000 | ps | 1 |

See "Single-ended Test Loads Page" for termination circuits

¹Guaranteed by design and characterization, not 100% tested in production.

²Measured between 0.8V and 2.0V

Clock AC Tolerances

| | SRC, NS_SAS | PCI | DOT96 | 48MHz | REF | |
|-----------------------|----------------|--------|-------|-------|-------|-----|
| PPM tolerance | 100 | 100 | 100 | 100 | 100 | ppm |
| Cycle to Cycle Jitter | 50 | 500 | 250 | 350 | 1000 | ps |
| Spread | -0.50% | -0.50% | 0 | 0.00% | 0.00% | % |

Clock Periods – Outputs with Spread Spectrum Disabled

| SSC ON | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|----------------|------------------------|------------------------------|--------------------------------------|--------------------------------------|-------------------------|--------------------------------------|--------------------------------------|------------------------------|-------|-------|
| | | 1 Clock | 1 us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| SRC, NS_SAS | 100.00000 | 9.94900 | | 9.99900 | 10.00000 | 10.00100 | | 10.05100 | ns | 1,2 |
| PCI | 33.33333 | 29.49700 | | 29.99700 | 30.00000 | 30.00300 | | 30.50300 | ns | 1,2 |
| DOT96 | 96.00000 | 10.16563 | | 10.41563 | 10.41667 | 10.41771 | | 10.66771 | ns | 1,2 |
| 48MHz | 48.00000 | 20.48125 | | 20.83125 | 20.83333 | 20.83542 | | 21.18542 | ns | 1,2 |
| REF | 14.31818 | 69.78429 | | 69.83429 | 69.84128 | 69.84826 | | 69.89826 | ns | 1,2 |

Clock Periods – Outputs with Spread Spectrum Enabled

| SSC ON | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|--------|------------------------|------------------------------|--------------------------------------|--------------------------------------|-------------------------|--------------------------------------|--------------------------------------|------------------------------|-------|-------|
| | | 1 Clock | 1 us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| PCI | 33.25 | 29.49718 | 29.99718 | 30.07218 | 30.07519 | 30.07820 | 30.15320 | 30.65320 | ns | 1,2 |
| SRC | 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.10107 | ns | 1,2 |

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy specifications are guaranteed with the assumption that the REF output is tuned to exactly 14.31818MHz.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | |
|-----------------------------|-----------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| Beginning Byte = N | | ACK |
| Data Byte Count = X | | ACK |
| Beginning Byte N | | ACK |
| O | X Byte | O |
| O | | O |
| O | | O |
| Byte N + X - 1 | | ACK |
| P | stoP bit | |

SMBus write address = D2 hex

SMBus read address = D3 hex

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | |
|----------------------------|-----------------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| Beginning Byte = N | | ACK |
| Repeat starT | | ACK |
| Slave Address | | |
| RD | ReaD | |
| Data Byte Count=X | | ACK |
| Beginning Byte N | | ACK |
| ACK | | O |
| ACK | | O |
| O | | O |
| O | | |
| Byte N + X - 1 | | |
| N | Not acknowledge | |
| P | stoP bit | |

SMBus Table: Output Enable Register

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------------|------------------|------|--------------|--------|---------|
| Bit 7 | - | DOT96 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 6 | - | NS_SAS1 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 5 | | RESERVED | | | | | 1 |
| Bit 4 | - | NS_SAS0 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 3 | | RESERVED | | | | | 1 |
| Bit 2 | - | SRC2 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 1 | - | SRC1 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 0 | - | SRC0 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |

SMBus Table: Output Enable Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|---------|------------------------|------------------|------|-------------|-----------|---------|
| Bit 7 | - | REF14_3x Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 6 | | RESERVED | | | | | 0 |
| Bit 5 | | RESERVED | | | | | 0 |
| Bit 4 | | RESERVED | | | | | 1 |
| Bit 3 | | RESERVED | | | | | 1 |
| Bit 2 | | RESERVED | | | | | 1 |
| Bit 1 | | RESERVED | | | | | 1 |
| Bit 0 | SRC/PCI | Spread Spectrum Enable | Spread Off/On | RW | Spread Off | Spread On | 0 |

SMBus Table: Output Enable Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|--------------|------------------|------|-------------|--------|---------|
| Bit 7 | | RESERVED | | | | | 0 |
| Bit 6 | | RESERVED | | | | | 0 |
| Bit 5 | - | PCI4 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 4 | - | PCI3 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 3 | - | PCI2 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 2 | - | PCI1 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 1 | - | PCI0 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 0 | - | 48MHz Enable | Output Enable | RW | Disable-Low | Enable | 1 |

Byte 3 ~ Byte 4 Reserved Register

SMBus Table: NS_SAS Frequency Margining Table

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|------------------|------|----------------------------|---|---------|
| Bit 7 | | RESERVED | | | | | 0 |
| Bit 6 | | RESERVED | | | | | 0 |
| Bit 5 | | RESERVED | | | | | 0 |
| Bit 4 | - | FS4 | Freq. Sel 4 | RW | See NS_SAS Frequency Table | | 0 |
| Bit 3 | - | FS3 | Freq. Sel 3 | RW | | 1 | |
| Bit 2 | - | FS2 | Freq. Sel 2 | RW | | 1 | |
| Bit 1 | - | FS1 | Freq. Sel 1 | RW | | 1 | |
| Bit 0 | - | FS0 | Freq. Sel 0 | RW | | 1 | |

SMBus Table: SRC/PCI Frequency Select Register

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|------------------|------|------------------------------------|---|---------|
| Bit 7 | - | RESERVED | | | | | 0 |
| Bit 6 | - | RESERVED | | | | | 0 |
| Bit 5 | - | RESERVED | | | | | 0 |
| Bit 4 | - | RESERVED | | | | | 1 |
| Bit 3 | - | FS3 | Freq. Sel 3 | RW | See SRC/PCI Frequency Select Table | | 1 |
| Bit 2 | - | FS2 | Freq. Sel 2 | RW | | 0 | |
| Bit 1 | - | FS1 | Freq. Sel 1 | RW | | 0 | |
| Bit 0 | - | FS0 | Freq. Sel 0 | RW | | 0 | |

SMBus Table: Vendor & Revision ID Register

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|------------------|---|---------|
| Bit 7 | - | RID3 | REVISION ID | R | 0011 for A rev | | 0 |
| Bit 6 | - | RID2 | | R | | | 0 |
| Bit 5 | - | RID1 | | R | | | 1 |
| Bit 4 | - | RID0 | | R | | | 1 |
| Bit 3 | - | VID3 | VENDOR ID | R | 0001 for ICS/IDT | | 0 |
| Bit 2 | - | VID2 | | R | | | 0 |
| Bit 1 | - | VID1 | | R | | | 0 |
| Bit 0 | - | VID0 | | R | | | 1 |

SMBus Table: Byte Count Register

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|----------------------------------|------|--|---|---------|
| Bit 7 | - | BC7 | Byte Count Programming b(7:0) | RW | Writing to this register will configure how many bytes will be read back, default is A bytes (0 to 9) | | 0 |
| Bit 6 | - | BC6 | | RW | | | 0 |
| Bit 5 | - | BC5 | | RW | | | 0 |
| Bit 4 | - | BC4 | | RW | | | 0 |
| Bit 3 | - | BC3 | | RW | | | 1 |
| Bit 2 | - | BC2 | | RW | | | 0 |
| Bit 1 | - | BC1 | | RW | | | 1 |
| Bit 0 | - | BC0 | | RW | | | 0 |

SMBus Table: Device ID Register

| Byte 9 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|-----------------------|------|---|---|---------|
| Bit 7 | | DID7 | Device ID (17 hex) | R | - | - | 0 |
| Bit 6 | | DID6 | | R | - | - | 0 |
| Bit 5 | | DID5 | | R | - | - | 0 |
| Bit 4 | | DID4 | | R | - | - | 1 |
| Bit 3 | | DID3 | | R | - | - | 0 |
| Bit 2 | | DID2 | | R | - | - | 1 |
| Bit 1 | | DID1 | | R | - | - | 1 |
| Bit 0 | | DID0 | | R | - | - | 1 |

SMBus Table: M/N Programming & Control Register

| Byte 10 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------|--------|----------------------------------|------|---------|--------|---------|
| Bit 7 | - | M/N_EN | SRC M/N Programming Enable | RW | Disable | Enable | 0 |
| Bit 6 | - | | RESERVED | | | | 0 |
| Bit 5 | - | | RESERVED | | | | 0 |
| Bit 4 | - | | RESERVED | | | | 0 |
| Bit 3 | - | | RESERVED | | | | 0 |
| Bit 2 | - | | RESERVED | | | | 0 |
| Bit 1 | - | | RESERVED | | | | 0 |
| Bit 0 | - | | RESERVED | | | | 0 |

SMBus Table: SRC/PCI Frequency Control Register

| Byte 11 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------|------------|------------------------------------|------|--|---|---------|
| Bit 7 | - | SRC N Div8 | N Divider Prog bit 8 | RW | The decimal representation of M and N Divider in Byte 11 and 12 will configure the SRC VCO frequency. Default at power up = latch-in or Byte 6 Rom table. VCO Frequency = $25 \times [N\text{Div}(9:0)+8] /$ $[M\text{Div}(5:0)+2]$ | | X |
| Bit 6 | - | SRC N Div9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | - | SRC M Div5 | M Divider Programming bit (5:0) | RW | | | X |
| Bit 4 | - | SRC M Div4 | | RW | | | X |
| Bit 3 | - | SRC M Div3 | | RW | | | X |
| Bit 2 | - | SRC M Div2 | | RW | | | X |
| Bit 1 | - | SRC M Div1 | | RW | | | X |
| Bit 0 | - | SRC M Div0 | | RW | | | X |

SMBus Table: SRC Frequency Control Register

| Byte 12 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------|------------|---|------|---|---|---------|
| Bit 7 | - | SRC N Div7 | N Divider Programming Byte12 bit(7:0) and Byte11 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 11 and 12 will configure the SRC VCO frequency. Default at power up = latch-in or Byte 6 Rom table. VCO Frequency = 25 x [NDiv(9:0)+8] / [MDiv(5:0)+2] | | X |
| Bit 6 | - | SRC N Div6 | | RW | | | X |
| Bit 5 | - | SRC N Div5 | | RW | | | X |
| Bit 4 | - | SRC N Div4 | | RW | | | X |
| Bit 3 | - | SRC N Div3 | | RW | | | X |
| Bit 2 | - | SRC N Div2 | | RW | | | X |
| Bit 1 | - | SRC N Div1 | | RW | | | X |
| Bit 0 | - | SRC N Div0 | | RW | | | X |

SMBus Table: SRC Spread Spectrum Control Register

| Byte 13 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------|----------|---|------|--|---|---------|
| Bit 7 | - | SRC SSP7 | Spread Spectrum Programming bit(7:0) | RW | These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of SRC | | X |
| Bit 6 | - | SRC SSP6 | | RW | | | X |
| Bit 5 | - | SRC SSP5 | | RW | | | X |
| Bit 4 | - | SRC SSP4 | | RW | | | X |
| Bit 3 | - | SRC SSP3 | | RW | | | X |
| Bit 2 | - | SRC SSP2 | | RW | | | X |
| Bit 1 | - | SRC SSP1 | | RW | | | X |
| Bit 0 | - | SRC SSP0 | | RW | | | X |

SMBus Table: SRC Spread Spectrum Control Register

| Byte 14 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------|-----------|--|------|--|---|---------|
| Bit 7 | - | | Reserved | | | | 0 |
| Bit 6 | - | SRC SSP14 | Spread Spectrum Programming bit(14:8) | RW | These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of SRC | | X |
| Bit 5 | - | SRC SSP13 | | RW | | | X |
| Bit 4 | - | SRC SSP12 | | RW | | | X |
| Bit 3 | - | SRC SSP11 | | RW | | | X |
| Bit 2 | - | SRC SSP10 | | RW | | | X |
| Bit 1 | - | SRC SSP9 | | RW | | | X |
| Bit 0 | - | SRC SSP8 | | RW | | | X |

SMBus Table: NS_SAS Frequency Control Register

| Byte 15 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------|---------------|---|------|--|---|---------|
| Bit 7 | - | NS_SAS N Div8 | N Divider Prog bit 8 | RW | The decimal representation of M and N Divider in Byte 15 and 16 will configure the NS_SAS VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 25 x [NDiv(9:0)+8] / [MDiv(5:0)+2] | | X |
| Bit 6 | - | NS_SAS N Div9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | - | NS_SAS M Div5 | M Divider Programming bits (Fixed at 1 for Rev D) | RW | | | X |
| Bit 4 | - | NS_SAS M Div4 | | RW | | | X |
| Bit 3 | - | NS_SAS M Div3 | | RW | | | X |
| Bit 2 | - | NS_SAS M Div2 | | RW | | | X |
| Bit 1 | - | NS_SAS M Div1 | | RW | | | X |
| Bit 0 | - | NS_SAS M Div0 | | RW | | | X |

SMBus Table: NS_SAS Frequency Control Register

| Byte 16 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------|---------------|---------------------------------|------|--|---|---------|
| Bit 7 | - | NS_SAS N Div7 | N Divider Programming b(7:0) | RW | The decimal representation of M and N Divider in Byte 15 and 16 will configure the NS_SAS VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 25 x [NDiv(9:0)+8] / [MDiv(5:0)+2] | | X |
| Bit 6 | - | NS_SAS N Div6 | | RW | | | X |
| Bit 5 | - | NS_SAS N Div5 | | RW | | | X |
| Bit 4 | - | NS_SAS N Div4 | | RW | | | X |
| Bit 3 | - | NS_SAS N Div3 | | RW | | | X |
| Bit 2 | - | NS_SAS N Div2 | | RW | | | X |
| Bit 1 | - | NS_SAS N Div1 | | RW | | | X |
| Bit 0 | - | NS_SAS N Div0 | | RW | | | X |

SRC/PCI Frequency Selection Table

| Line | Byte 1, Bit 0 Spread Enable | Byte6 Bit3 FS3 | Byte6 Bit2 FS2 | Byte6 Bit1 FS1 | Byte6 Bit0 FS0 | SRC (MHz) | PCI (MHz) | Spread % |
|------|--------------------------------------|----------------------|----------------------|----------------------|----------------------|---------------|--------------|-------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 89.97 | 29.99 | 0% |
| 1 | 0 | 0 | 0 | 0 | 1 | 91.28 | 30.43 | |
| 2 | 0 | 0 | 0 | 1 | 0 | 92.58 | 30.86 | |
| 3 | 0 | 0 | 0 | 1 | 1 | 93.75 | 31.25 | |
| 4 | 0 | 0 | 1 | 0 | 0 | 95.05 | 31.68 | |
| 5 | 0 | 0 | 1 | 0 | 1 | 96.22 | 32.07 | |
| 6 | 0 | 0 | 1 | 1 | 0 | 97.53 | 32.51 | |
| 7 | 0 | 0 | 1 | 1 | 1 | 98.83 | 32.94 | |
| 8 | 0 | 1 | 0 | 0 | 0 | 100.00 | 33.33 | |
| 9 | 0 | 1 | 0 | 0 | 1 | 101.30 | 33.77 | |
| 10 | 0 | 1 | 0 | 1 | 0 | 102.47 | 34.16 | |
| 11 | 0 | 1 | 0 | 1 | 1 | 103.78 | 34.59 | |
| 12 | 0 | 1 | 1 | 0 | 0 | 105.08 | 35.03 | |
| 13 | 0 | 1 | 1 | 0 | 1 | 106.25 | 35.42 | |
| 14 | 0 | 1 | 1 | 1 | 0 | 107.55 | 35.85 | |
| 15 | 0 | 1 | 1 | 1 | 1 | 110.03 | 36.68 | |
| 16 | 1 | 0 | 0 | 0 | 0 | 89.97 | 29.99 | -0.5% |
| 17 | 1 | 0 | 0 | 0 | 1 | 91.28 | 30.43 | |
| 18 | 1 | 0 | 0 | 1 | 0 | 92.58 | 30.86 | |
| 19 | 1 | 0 | 0 | 1 | 1 | 93.75 | 31.25 | |
| 20 | 1 | 0 | 1 | 0 | 0 | 95.05 | 31.68 | |
| 21 | 1 | 0 | 1 | 0 | 1 | 96.22 | 32.07 | |
| 22 | 1 | 0 | 1 | 1 | 0 | 97.53 | 32.51 | |
| 23 | 1 | 0 | 1 | 1 | 1 | 98.83 | 32.94 | |
| 24 | 1 | 1 | 0 | 0 | 0 | 100.00 | 33.33 | |
| 25 | 1 | 1 | 0 | 0 | 1 | 101.30 | 33.77 | |
| 26 | 1 | 1 | 0 | 1 | 0 | 102.47 | 34.16 | |
| 27 | 1 | 1 | 0 | 1 | 1 | 103.78 | 34.59 | |
| 28 | 1 | 1 | 1 | 0 | 0 | 105.08 | 35.03 | |
| 29 | 1 | 1 | 1 | 0 | 1 | 106.25 | 35.42 | |
| 30 | 1 | 1 | 1 | 1 | 0 | 107.55 | 35.85 | |
| 31 | 1 | 1 | 1 | 1 | 1 | 110.03 | 36.68 | |

NS_SAS Margining Table

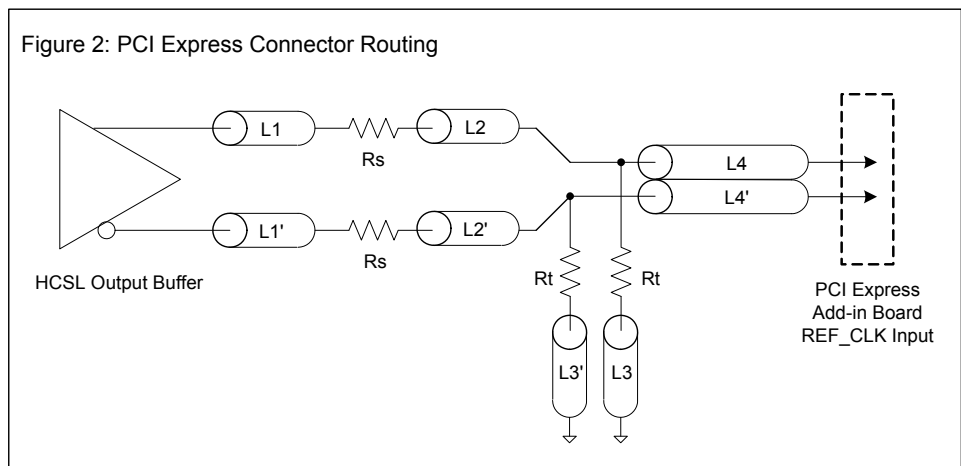
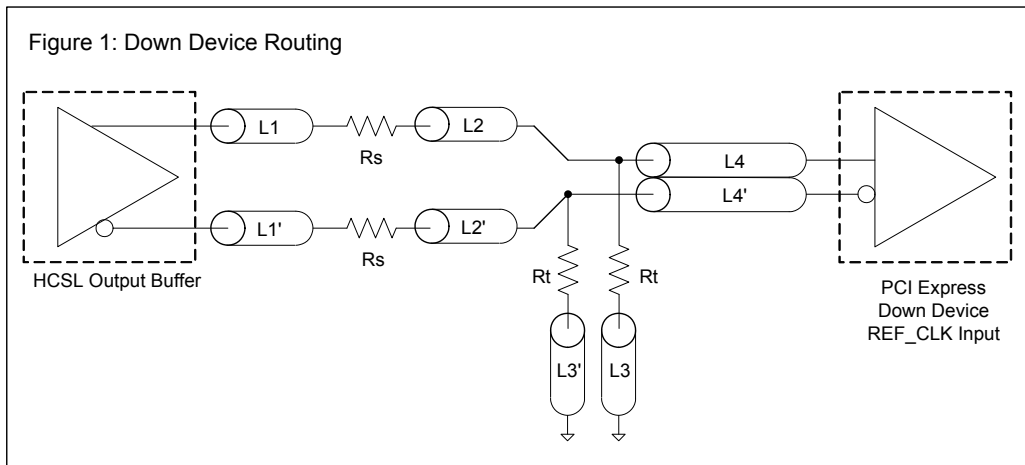
| Line | Byte5 Bit4 FS4 | Byte5 Bit3 FS3 | Byte5 Bit2 FS2 | Byte5 Bit1 FS1 | Byte5 Bit0 FS0 | NS_xxx (MHz) |
|------|----------------------|----------------------|----------------------|----------------------|----------------------|-----------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 58.33 |
| 1 | 0 | 0 | 0 | 0 | 1 | 61.11 |
| 2 | 0 | 0 | 0 | 1 | 0 | 63.89 |
| 3 | 0 | 0 | 0 | 1 | 1 | 66.67 |
| 4 | 0 | 0 | 1 | 0 | 0 | 69.44 |
| 5 | 0 | 0 | 1 | 0 | 1 | 72.22 |
| 6 | 0 | 0 | 1 | 1 | 0 | 75.00 |
| 7 | 0 | 0 | 1 | 1 | 1 | 77.78 |
| 8 | 0 | 1 | 0 | 0 | 0 | 80.56 |
| 9 | 0 | 1 | 0 | 0 | 1 | 83.33 |
| 10 | 0 | 1 | 0 | 1 | 0 | 86.11 |
| 11 | 0 | 1 | 0 | 1 | 1 | 88.89 |
| 12 | 0 | 1 | 1 | 0 | 0 | 91.67 |
| 13 | 0 | 1 | 1 | 0 | 1 | 94.44 |
| 14 | 0 | 1 | 1 | 1 | 0 | 97.22 |
| 15 | 0 | 1 | 1 | 1 | 1 | 100.00 |
| 16 | 1 | 0 | 0 | 0 | 0 | 102.78 |
| 17 | 1 | 0 | 0 | 0 | 1 | 105.56 |
| 18 | 1 | 0 | 0 | 1 | 0 | 108.33 |
| 19 | 1 | 0 | 0 | 1 | 1 | 111.11 |
| 20 | 1 | 0 | 1 | 0 | 0 | 113.89 |
| 21 | 1 | 0 | 1 | 0 | 1 | 116.67 |
| 22 | 1 | 0 | 1 | 1 | 0 | 119.44 |
| 23 | 1 | 0 | 1 | 1 | 1 | 122.22 |
| 24 | 1 | 1 | 0 | 0 | 0 | 125.00 |
| 25 | 1 | 1 | 0 | 0 | 1 | 127.78 |
| 26 | 1 | 1 | 0 | 1 | 0 | 130.56 |
| 27 | 1 | 1 | 0 | 1 | 1 | 133.33 |
| 28 | 1 | 1 | 1 | 0 | 0 | 136.11 |
| 29 | 1 | 1 | 1 | 0 | 1 | 138.89 |
| 30 | 1 | 1 | 1 | 1 | 0 | 141.67 |
| 31 | 1 | 1 | 1 | 1 | 1 | 144.44 |

NOTE: Operation at other than the default entry is not guaranteed. These values are for margining purposes only.

| DIF Reference Clock | | | |
|---|--------------------|------|--------|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace | 0.5 max | inch | 1 |
| L2 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| L3 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| R_s | 33 | ohm | 1 |
| R_t | 49.9 | ohm | 1 |

| Down Device Differential Routing | | | |
|--|---------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace | 1.8 min to 14.4 max | inch | 1 |

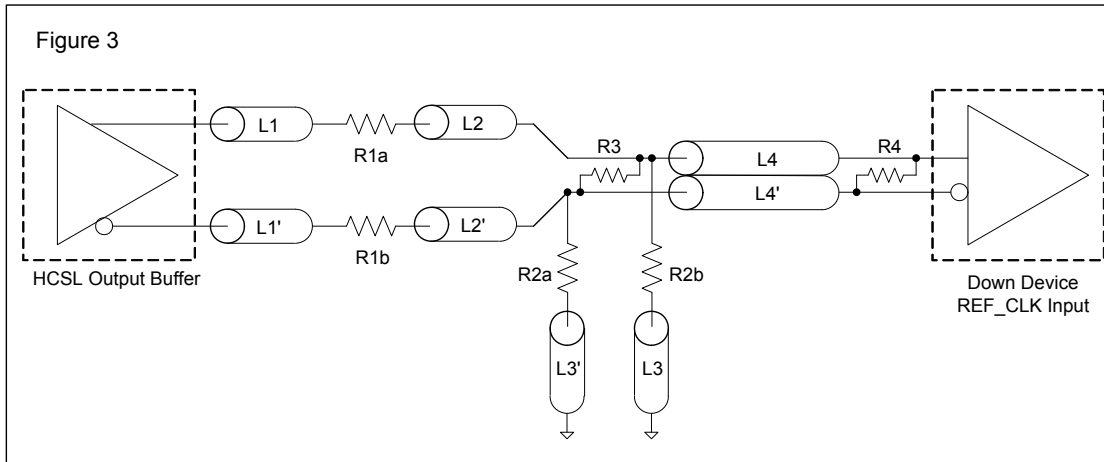
| Differential Routing to PCI Express Connector | | | |
|--|-----------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace | 0.225 min to 12.6 max | inch | 2 |



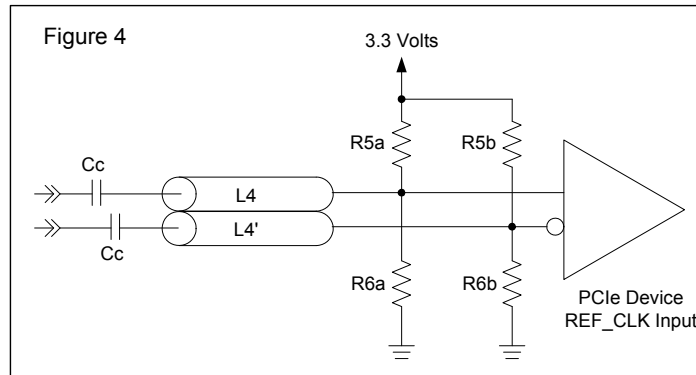
| Alternative Termination for LVDS and other Common Differential Signals (figure 3) | | | | | | | |
|---|-------|------|----|------|------|-----|--------------------------------|
| Vdiff | Vp-p | Vcm | R1 | R2 | R3 | R4 | Note |
| 0.45v | 0.22v | 1.08 | 33 | 150 | 100 | 100 | |
| 0.58 | 0.28 | 0.6 | 33 | 78.7 | 137 | 100 | |
| 0.80 | 0.40 | 0.6 | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60 | 0.3 | 1.2 | 33 | 174 | 140 | 100 | Standard LVDS |

R1a = R1b = R1

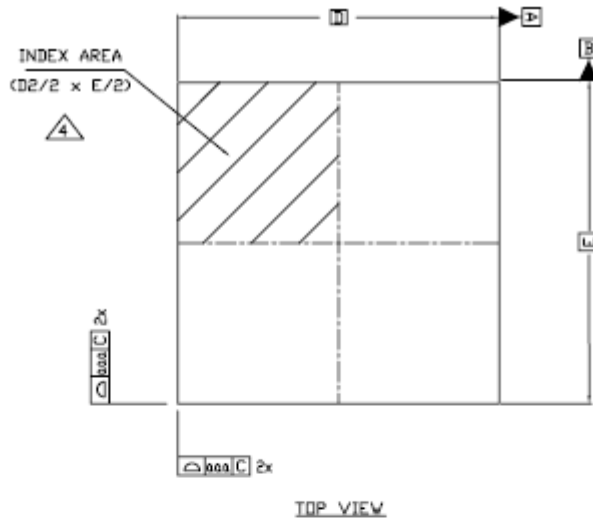
R2a = R2b = R2



| Cable Connected AC Coupled Application (figure 4) | | |
|---|-------------|------|
| Component | Value | Note |
| R5a, R5b | 8.2K 5% | |
| R6a, R6b | 1K 5% | |
| Cc | 0.1 μ F | |
| Vcm | 0.350 volts | |



Package Outline and Package Dimensions (48-pin MLF)



| SYMBOL | DIMENSION | | |
|--------|-----------|----------|------|
| | MIN | NOM | MAX |
| D2 | 3.95 | 4.10 | 4.20 |
| E2 | 3.95 | 4.10 | 4.20 |
| L | 0.30 | 0.40 | 0.50 |
| D | 6.00 BSC | | |
| E | 6.00 BSC | | |
| e | 0.40 BSC | | |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | --- | 0.20 ref | --- |
| N | 48 | | |
| ND | 12 | | |
| NE | 12 | | |
| b | .15 | .20 | .25 |

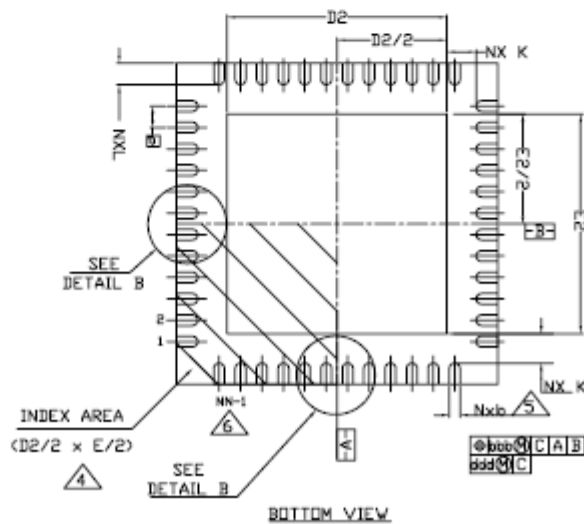
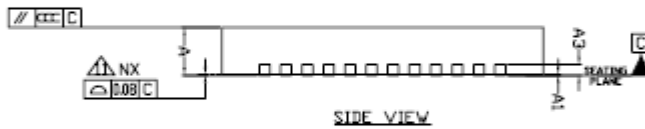
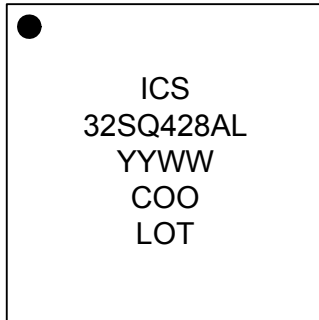


FIGURE 1
B 9

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N REFERS TO THE NUMBER OF LEADS.
4. ND AND NE REFER TO THE NUMBER OF LEADS PER SIDE.

Marking Diagram



Notes:

1. 'L' denotes RoHS compliant package.
2. 'YYWW' is the date code.
3. 'COO' is the country of origin.
4. 'LOT' is the lot number.

Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---------------------|--------------------|------------|-------------|
| 932SQ428AKLF | Tray | 48-pin MLF | 0 to +70° C |
| 932SQ428AKLFT | Tape and Reel | 48-pin MLF | 0 to +70° C |

"LF" suffix to the part number are the Pb-Free configuration, RoHS compliant.

"A" is the device revision designator (will not correlate with the datasheet revision).

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Revision History

| Rev. | Issue Date | Who | Description | Page # |
|------|------------|-----|---|--------|
| A | 4/15/2011 | RDW | Updated Idd, phase jitter, minor typo corrections; released to final | |
| B | 7/26/2011 | RDW | Updated Power Down Functionality table to clarify functionality of single-ended outputs in power down. | |
| C | 12/8/2011 | RDW | 1. Updated Phase Jitter Table to correct typo in "Conditions" column for SAS. 2. Mark spec added. | 8, 21 |
| D | 4/13/2012 | AT | Typo on pin 40 description. Pin type states OUT; should be IN | 4 |
| E | 4/23/2012 | RDW | Updated Rp values on Output Terminations Table from 43.2 ohms to 42.2 or 43.2 ohms to be consistent with Intel. | 5 |

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