



PIC18F1230/1330

PIC18F1230/1330 Rev. A4 Silicon Errata

The PIC18F1230/1330 Rev. A4 parts you have received conform functionally to the Device Data Sheet (DS39758C), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F1230/1330 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F1230/1330 devices with these Device/Revision IDs:

| Part Number | Device ID | Revision ID |
|-------------|---------------|-------------|
| PIC18F1230 | 0001 1110 000 | 0 0101 |
| PIC18F1330 | 0001 1110 001 | 0 0101 |

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

All of the issues listed here will be addressed in future revisions of the PIC18F1230/1330 silicon.

1. Module: Comparator

The CMPxIF flag, which indicates when each comparator has a switched state, cannot be cleared immediately after reading CMCON. The mismatch condition that sets CMPxIF persists for 1 T_{cy} after reading/writing CMCON.

Work around

Insert a NOP instruction between reading/writing CMCON and clearing the CMPxIF flag.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In Synchronous Slave Transmission mode, the TRMT bit (TXSTA<1>) may not indicate when the TSR register is empty.

Work around

Instead of polling the TRMT bit to determine the status of the EUSART, poll the TXIF flag (PIR1<4>) to determine when new data can be written to the TXREG register.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations, one or more extra bytes have been observed in a packet transmitted by the module operating in Asynchronous mode. The actual data is not lost or corrupted – only extra bytes are added. The extra bytes may be 0x00 or 0xFF.

This situation occurs when the contents of the transmit buffer (TXREG) are transferred to the TSR at the end of the Stop bit period at the same time that firmware writes to TXREG.

Note that TXIF is set at the beginning of the Stop bit period.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

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4. Module: Comparator Voltage Reference

The comparator voltage reference module (CVREF) does not offer the option of bypassing the CVREF module.

The CVREF module offers the option of providing the following inputs to the comparators:

- Scaled VDD
- Scaled VREF
- No reference (disabled)

Table 1 shows how the CVREN and CVRSS bits are configured to enable the options.

TABLE 1: VOLTAGE REFERENCE OUTPUT

| CVREN CVRCON<7> | CVRSS CVRCON<4> | Comparator Reference |
|--------------------|--------------------|-------------------------|
| 0 | x (don't care) | Disabled |
| 1 | 0 | CVREF uses AVDD |
| 1 | 1 | CVREF uses VREF |

5. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (the SPEN bit, RCSTA <7> = 0)
- The EUSART is re-enabled (RCSTA <7> = 1)
- A two-cycle instruction is executed

Work around

Add a 2 T_{cy} delay after re-enabling the EUSART.

1. Disable Receive Interrupts (RCIE bit, PIE1<5> = 0).
2. Disable the EUSART (RCSTA <7> = 0).
3. Re-enable the EUSART (RCSTA <7> = 1).
4. Re-enable receive interrupts (PIE1<5> = 1).
(This is the first T_{cy} delay.)
5. Execute a NOP instruction.
(This is the second T_{cy} delay.)

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (3/2007)

First revision of this document. Includes silicon issues 1 (Comparator) and 2-3 (EUSART).

Rev B Document (7/2007)

Silicon issues 1 (Comparator) and 2-3 (EUSART) were rewritten and document format was corrected.

Rev C Document (1/2008)

Added silicon issue 4 (Comparator Voltage Reference).

Rev D Document (12/2008)

Added silicon issue 5 (Enhanced Universal Synchronous Asynchronous Receiver Transmitter – EUSART).

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NOTES:

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