

# Enpirion EN5396QI 9A DCDC Converter w/Integrated Inductor Evaluation Board

## Introduction

Thank you for choosing Altera Enpirion power products!

- The EN5396QI features integrated inductor, power MOSFETS, Controller, Compensation Network, and protection circuitry against system faults. This level of integration delivers a substantial reduction in footprint and part count over competing solutions. However, the evaluation board is not optimized for minimum footprint; rather for engineering ease of evaluation through programming options, clip leads, test points etc.
- The EN5396QI features a customer programmable output voltage by means of a resistor divider. The resistor divider allows the user to set the output voltage to any value within the range 0.75V to  $(V_{IN}-V_{DROPOUT})$ . The evaluation board, as shipped is populated with a fixed resistor divider of 2k $\Omega$  (1%) each, for an output = 1.5Volts. The user may wish to use a different value for the upper resistor (R6) or even a potentiometer (R2) in lieu of the discrete resistor divider, to realize a different output voltage. The External Feedback (XFB) node is required to be low impedance to push the pole formed at this node to a high frequency (>5MHz.)
- The Over-Voltage-Protection (OVP) trip level is programmable using a separate resistor divider (R4 and R5.) The board does NOT come populated with the OVP resistors and the boards as shipped have no over voltage protection.
- The input capacitor is a 10V rated 2X47uF X5R MLCC. The output filter section is populated with 5 x 22uF, 6.3V rated X5R MLC capacitors to achieve the required ~100uF of output capacitance. The combination of 5 x 22uF caps yields very low ESR and hence low output ripple. 2X47uF capacitor may be substituted if minimizing footprint is more important. The Soft-start capacitor is a small 10V rated 15nF X5R MLCC.
- Pads are available to add an additional input capacitor and there are a total of 5 pads to accommodate the output capacitor(s). This allows for evaluation of performance over a wide range of input/output capacitor combinations.
- A jumper is provided for controlling the Enable signal. Enable may also be controlled using an external switching source by removing the jumper and applying the enable signal to the middle pin and ground.

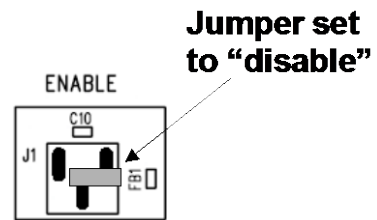
- Numerous test points are provided as well as banana plugs for input and output connections
- The board comes with input decoupling and reverse polarity protection to guard the device against common setup mishaps.

## Quick Start Guide

Figure 1 shows a top view of the evaluation board.

**WARNING:** complete steps 1 through 4 before applying power to the EN5396QI evaluation board.

**STEP 1:** Set the “ENABLE” jumper to the Disable Position.



**STEP 2:** Connect Power Supply to the input power connectors, VIN (+) and GND (-) as indicated in Figure 1 and set the supply to the desired voltage.

**CAUTION:** be mindful of the polarity. Even though the evaluation board comes with reverse polarity protection diodes, it is rarely a good idea to reverse the input polarity.

**STEP 3:** Connect the load to the output connectors VOUT (+) and GND (-), as indicated in Figure 1.

**STEP 4:** Apply  $V_{IN}$  to the board and move the ENABLE jumper to the enabled position. The EN5396QI is now powered up!

**STEP 4A: Power Up/Down Behavior** – Remove ENA jumper and connect a pulse generator (output disabled) signal to the middle pin of ENA and Ground. Set the pulse amplitude to go from 0 to 2.5 V. Set the pulse period to 10 msec. and duty cycle to 50%. Hook up oscilloscope probes to ENA, SS and VOUT with clean ground returns. Enable pulse generator output. Observe the SS capacitor and VOUT voltage ramps as ENA goes high and again as ENA goes low.

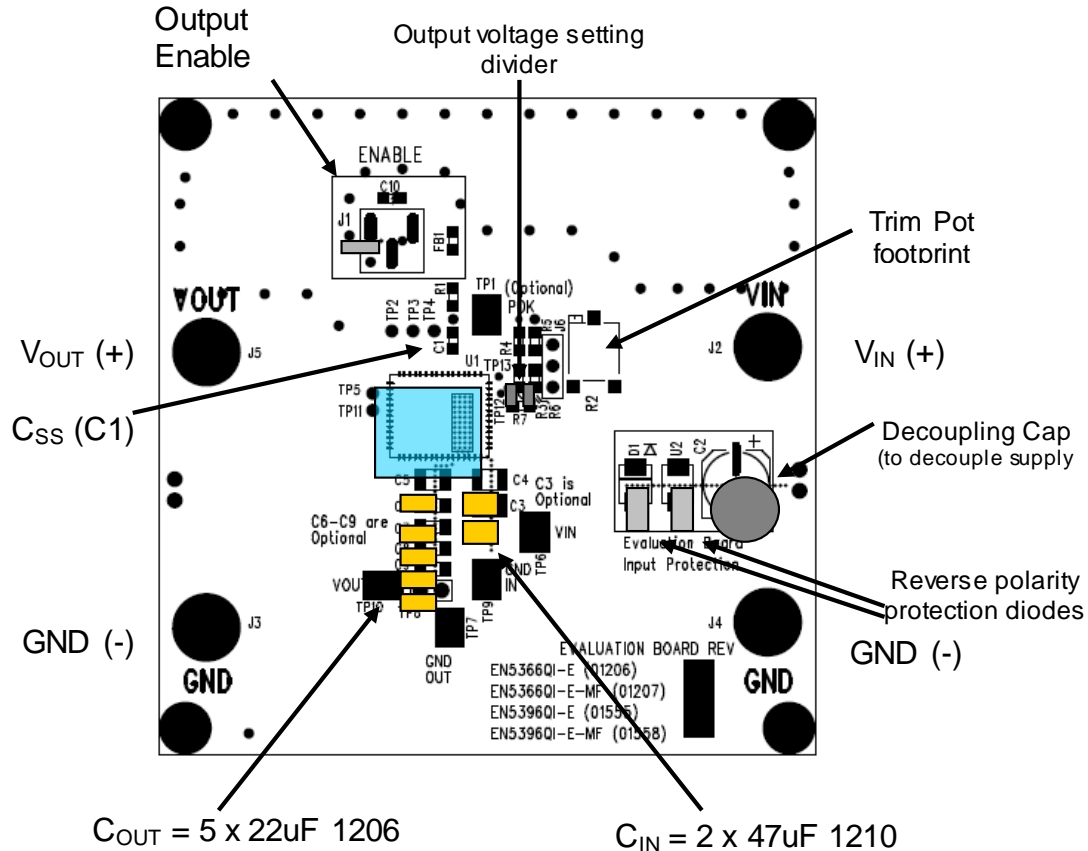


Figure 1. Evaluation Board Layout.

## Output Voltage Select

### Programming Output Voltage and OVP

The EN5396QI output voltage is programmed using a simple resistor divider network. Figure 2 shows a schematic view of the resistor divider configuration.

The EN5396QI output voltage and over voltage thresholds are determined by the voltages presented at the XFB and XOVP pins respectively. These voltages are set by way of resistor dividers between  $V_{OUT}$  and AGND with the midpoint going to XFB and XOVP.

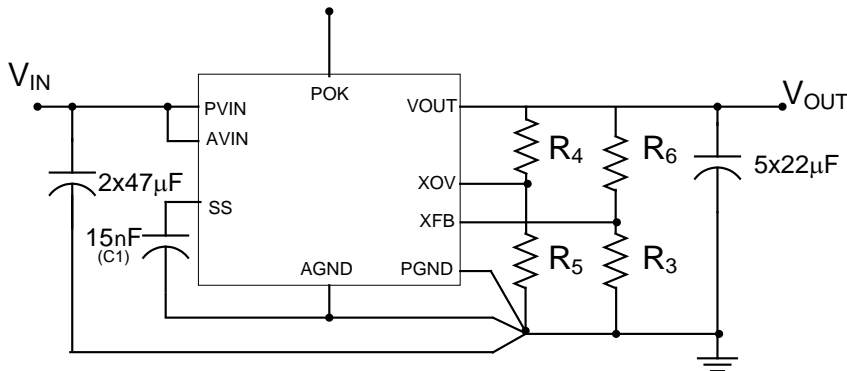
It is recommended that R3 and R5 resistor values be  $\sim 2k\Omega$ . Use the following equation to set the resistor R6 for the desired output voltage:

$$R6 = \frac{(V_{out} - 0.75V) * R3}{0.75V}$$

If over-voltage protection is desired, use the following equation to set the resistor R4 for the desired OVP trip-point. Note that the evaluation board leaves these resistors un-populated.

$$R4 = \frac{(OVP_{trip} - 0.90V) * R5}{0.90V}$$

By design, if both resistor dividers are the same, the OV trip-point will be 20% above the nominal output voltage.



**Figure 2.** V<sub>OUT</sub> and OVP resistor divider networks.

**NOTE:** if no OVP divider is present, there will be no over-voltage protection and POK will remain “high” as long as V<sub>OUT</sub> remains above 90% of the nominal V<sub>OUT</sub> setting.

## Test Recommendations

To guarantee measurement accuracy, the following precautions should be observed:

1. Make all input and output voltage measurements at the board using the test points provided. This will eliminate voltage drop across the line and load cables that can produce false readings.
2. Measure input and output current with series ammeters or accurate shunt resistors. This is especially important when measuring efficiency.
3. Use a balanced impedance probe tip to measure switching signals to avoid noise coupling into the probe ground lead. Output ripple and load transient deviation are best measured at TP8.
4. The board includes a 5.6k pull-up for the POK signal and ready to monitor the power OK status. The POK signal may be viewed at clip lead marked POK.
5. A 15nF soft-start capacitor is populated on the board for ~1msec soft-start time.

6. This evaluation board is not set up for paralleling multiple devices for greater load capability. A separate evaluation board is available that demonstrates a method for parallel operation of 2 EN5395Q1 devices.
7. The over-current protection circuit typically limits the maximum load current to approximately 1.5X the rated value – viz. 9A. However, this is somewhat adjustable via the ROCP pin. Please consult our Applications Engineering group for assistance in using this feature.
8. **DERATING:** The evaluation board may not be operated with maximum power dissipation (input power – output power) beyond a certain temperature (reference current derating curves in figure 3) for extended periods of time. The device will shut down when the internal junction temperature exceeds ~150°C.

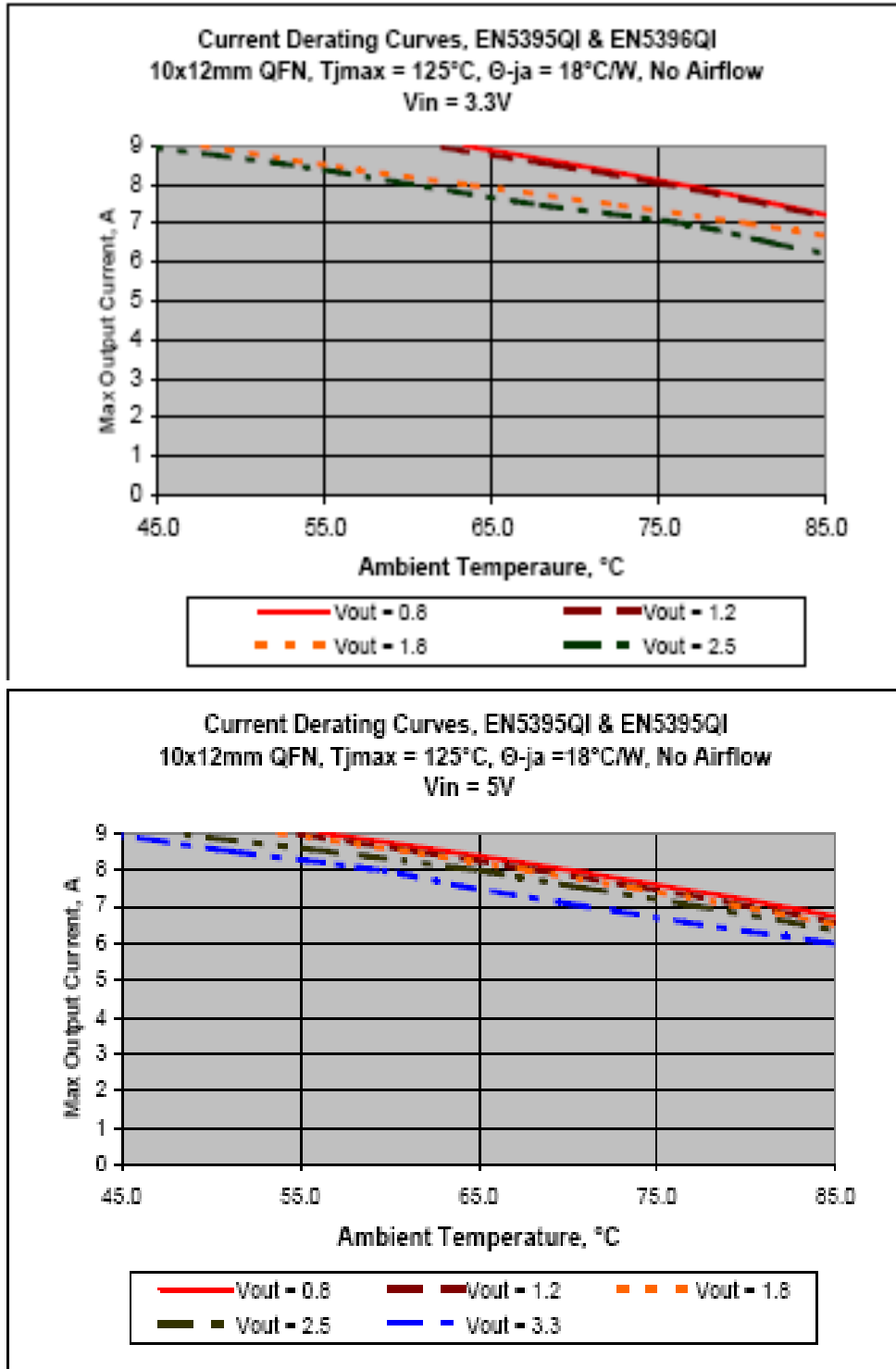


Figure 3. Current Derating Curves

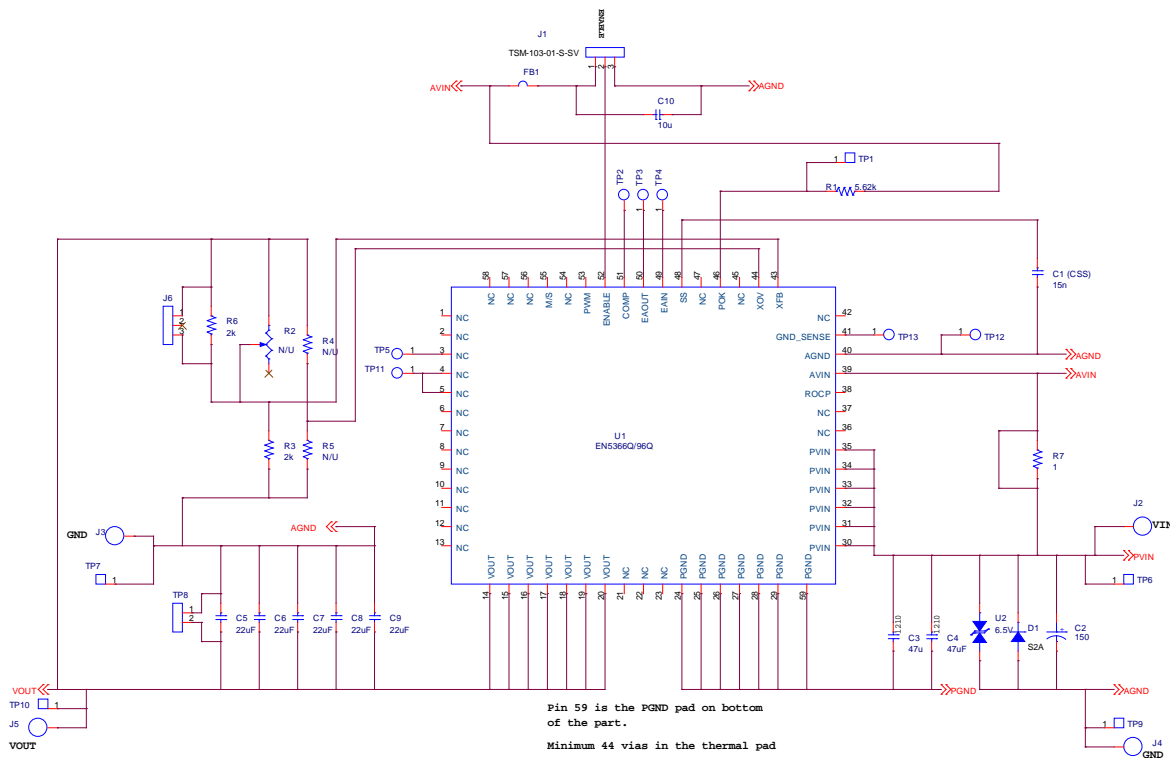
## Input and Output Capacitors

The **input** capacitance requirement is 2X47uF for the EN5396QI. Altera recommends that a low ESR MLC capacitor be used. The voltage rating should be rated high enough to provide adequate margin for your application. There is a pre-tinned pad for one additional 1210 capacitor to experiment with input filter performance.

The **output** capacitance requirement is approximately 100uF of capacitance. The EN5396QI-E evaluation board comes populated with 5 x 22uF, 6.3V 1206 MLC capacitors. The 5 parallel capacitors provide for reduced ESR and hence lower output ripple voltage. If a minimum footprint configuration is desired, the 5 x22uF capacitors can be replaced with 2X 47uF MLC capacitors.

**NOTE:** Capacitors must be X5R or X7R dielectric formulations.

**NOTE:** Please refer to product datasheet for specific recommendations.



## EN5396QI Evaluation Board Schematic



## Contact Information

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